Personnel Safety System Status Reporting via EPICS at the Advanced Photon Source^{*}

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ABSTRACT

The Personnel Safety System (PSS) for an experimental beamline at the Advanced Photon Source (APS) uses a dual-chain, PLC-based architecture for controlling shutters and experimental stations. Reporting the status of these two chains is important from both an operational and diagnostic standpoint. This paper discusses the methods used for passing information from both chains of the PSS to the EPICS-based control system at the APS.

I. INTRODUCTION

The design of the Personnel Safety System for the experimental beamlines at the Advanced Photon Source (APS) specifies the use of Programmable Logic Controllers (PLCs) for both interlock and control functions. To meet certain DOE requirements, the PSS was designed using two chains in an effort to avoid common-mode failures [1]. The first chain (denoted "Chain A") uses the Allen-Bradley PLC-5 series processor with both local and distributed I/O. The second chain ("Chain B") uses the GE/Fanuc 90-70 processor, also with both local and distributed I/O. Each beamline has its own autonomous PSS with no knowledge of, or communication with, any other beamline [2].

The (physical) size of the APS makes it necessary to be able to monitor the status of any given beamline from a remote location (such as the control room). To accomplish this without compromising the individuality of each PSS, special hardware and software has been added to both chains. These additions allow each chain to report a variety of information (including I/O points, status information, faults, etc.) to various EPICS database records. Once it is available as a collection of EPICS database records, any authorized X-Terminal or workstation has the ability to display the status of each beamline PSS. This information can be used for a variety of things including validation, debugging, fault tracing, and user training.

II. CONCEPTUAL DESIGN

The overall design requirements specified that the individual chain is responsible for sending the appropriate data to the EPICS database. It is also a requirement that the EPICS interface is not an integral function of the PSS operation (i.e., if the IOC goes down, the PSS must still function). Finally, it is also necessary that the communication be a read–only operation (the database must not have the ability to write into the PLC data space). Each chain has special hardware and software to meet these criteria.

III. CHAIN A - ALLEN-BRADLEY PLC-5

Allen-Bradley produces a VME "scanner" card that can be used to communicate with an Allen-Bradley back plane. This scanner typically connects via shielded twisted pair wire to an Allen-Bradley "Remote I/O Adapter," which sits in an Allen-Bradley crate. It is then possible to perform most of the functions of an Allen-Bradley PLC-5 processor – including reads and writes. Note that the "intelligence" of this system comes solely from the VME scanner – the Remote I/O Adapter is a non-intelligent device. At this point, it would seem that the simplest method of transferring data to EPICS from the PLCs would be to use this VME Scanner to Remote I/O Adapter communication. Two overriding concerns prevent this: firstly, the interlock system must be stand-alone and not dependent on the VME scanner, and secondly, any type of write operation (from the VME to the PLC) must not be allowed as it may compromise the integrity of the interlock program. A data transfer method that only <u>reads</u> from the Interlock System is

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required: a one-way communication that "filters" the data the VME side can access. To facilitate such a communication requires the use of an Allen-Bradley "Direct Communications Module" (DCM). This module was designed to allow a remote PLC processor to access the local processors data space (both read and write) through shielded, twisted pair cable ("blue hose"). The DCM occupies a slot in the same chassis as the local processor. Communication between the local processor and the DCM is done directly through the backplane. The local processor decides what data it wants the DCM to read and/or write. It is this ability that allows us to achieve the desired communication protocol [3].

It was decided to pass all of the input and output bits into EPICS, along with certain PLC status information, and a fault stack containing a time-ordered list of faults. To accomplish this, a small amount of code was added to the PSS logic that collects all of this data into two groups and sends them to the DCM via the Block Transfer construct. The DCM is configured to buffer the blocks (a block can be up to 64 words - 16 bits each) coming in over the (Allen-Bradley) backplane and send them over the blue hose when the VME scanner requests them. A new EPICS record type, denoted the "abDcm," is used to specify such parameters as the scanner address (in "Link, Rack, Slot" notation), number of word groups to read, and scan frequency. For each binary value (mostly input and output bits) a "bi" record is created for use in EPICS applications such as MEDM and the Alarm Handler. In an attempt to reduce network traffic, all binary input records are interrupt scanned [4].



FIGURE 1 - SCHEMATIC LAYOUT OF IOC AT SECTOR 2

Each IOC supports six beamlines (see figure 1). In order to maintain isolation between beamlines, six VME scanners are used (each with a different link number). The scan time for each DCM is fixed at one second, making the best-case resolution for updates about once per second (chain A).

IV. CHAIN B - GE/FANUC

General Electric makes a line of 90-70 coprocessors that sit on the GE backplane and are capable of running programs independently of the main processor. All main processor memory is available for inspection by the coprocessor, including I/O and status. We choose a coprocessor with configurable serial ports that can be programmed in a extended BASIC language, which GE named "MegaBasic". MegaBasic was chosen due to its large flexibility in controlling character output format to the serial ports, along with the relative ease of programming.

A small MegaBasic program was written that continuously scans the input, output, and status bits of the main processor, forms them into a string of hexadecimal characters, and prints them out of the serial port. A single frame consists of a start flag (the ASCII character "s"), the byte representation of the main processor memory, an end flag (letter "t"), and a checksum. Frames are sent continuously with no regard to acknowledgments. The serial port of the coprocessor is connected to a fiber-optic modem to allow long cable runs without (electical) noise problems. The other end of the fiber pair is connected to another fiber modem (one of many concentrated in a "serial 12" chassis - see figure 1), which in turn is connected to the VME module (described below).

On the VME side, a MVME162 module running the Hideos operating system is configured with two quad serial IP (Industry Pack) modules. Each of the IP modules is capable of communicating with four serial (RS-232) devices. The serial port of the GE co-processor is connected to one of the eight available serial ports on the MVME162 via fiber. A Hideos task was written to read the status frames arriving from the coprocessor and check for successful transmission (via the framing bits and the checksum). If a valid transmission is not received in five seconds of the last received frame, the connection is assumed dead and the record support specifies an invalid alarm.

Assuming a successful transmission, the Hideos task then looks at groups of two bytes (a "bitgroup") and checks to see if any bit has changed within a group. If so, the associated records within the bitgroup are signaled to the process and the values are updated appropriately [5]. As in the Allen-Bradley implementation, a separate binary input record is created to map each individual I/O point of the Chain B PSS.

Monitoring chain B takes only one MVME162 card since the IP modules allow us to connect to six individual GE coprocessors. The communication between the GE coprocessor and the MVME162 takes place at 19.2 Kbps. Assuming a low noise connection (which is valid since we are using fiber as the transmission medium), we will experience very few corrupted frames and can easily match the one second resolution of Chain A.

V. OPERATOR INTERFACE

MEDM was used to build a variety of screens (see figure 2). In general it was desired to be able to monitor all input and output points for both chains simultaneously. A special database was created to compare related outputs between chains and is used to flag abnormal conditions (for example, if an input does not appear on both chains when it is normally supposed to). Other screens include a fault stack (showing the last 10 faults), a PLC status page (showing a variety of PLC–specific information) and navigation (via menus).

Other screens show a schematic overview of the beamline and experimental stations. These screens are more useful to the experimenters to indicate status of shutters, doors, etc. (figure 3).

- Inp	utAB.3id.adl 🗾 🔹 🗖
3ID PSS CH	annel Input Overview
Sta	ations A and B 🛛 🖪
	Charles A
	Chain A
	Chain B
IPS1LS_OPENED IPS1LS_CLOSED	
IPSILS_CLOSED	IDRCTA_ADR3CLPB
	IDRCTA_ADR2LKPB
ISS1LS_OPENED	IDRCTA_ADR10PPB
ISS1LS_CLOSED	IDRCTA_ADR1CLPB
IPS2LS_CLOSED ISS1LS_OPENED ISS1LS_CLOSED ISS1XS_CLOSED ISS1XS_CLOSED	IDRCTA_BDR20PPB
ISS2LS_OPENED	IDRCTA_BDR2CLPB
ISS2LS_CLOSED —	IDRCTA_BDR1UNPB
ISS2XS_CLOSED 💳	IDRCTA_BDR1LKPB
IBLEPS_P5PERM	ISYSCT_MINORKEY
IBLEPS_P8CPERM	ISYSCT_MAJORKEY
IBLEPS_P8DPERM	ISTATA_DR3CLSD 🔂 🗖
IACIS_GLBONLN	ISTATA_DR3LCKD 📩
IACIS_FEPERM	ISTATA_DR2CLSD
IFEEPS_PS10PER IFEEPS_PS10PEN	ISTATA_DR2LCKD
IFEEPS_PS10PEN	ISTATA_DR1CLSD
ISHMAN_DISABLED	ISTATA_DR1LCKD
IFEEPS_FEPERM	ISTATA_SB2RSTPB
IWDTMR_FRMCHA/B	ISTATA_SB2CRSPB
IASRCHD_FRMCHA	ISTATA_SB1CRSPB
IBSRCHD_FRMCHA	ISTATB_DR2CLSD
ICSRCHD_FRMCHA	
IDSRCHD_FRMCHA	ISTATB_DR1CLSD
ISTCTA_ACTIVEPB 💼	ISTATB_DR1LCKD
ISTCTA_STNDBYPB	ISTATB_DRRCLSD 🔂
ISTCTA_ASHOPPB	ISTATB_SB2RSTPB 📩
ISTCTA_ASHCLPB	ISTATB_SB1RSTPB
ISTCTA_BSHOPPB	ISTATB_SB2CRSPB ISTATB_SB1CRSPB
ISTCTA_BSHCLPB	
_	IP5MS1_OPENED IP5MS1_CLOSED IP5MS2_OPENED
ISTCTA_AAPSKEY	IP5MS1_CLOSED
ISTCTA_BAPSKEY	IP5MS2_OPENED
	IP5MS2_CLOSED
	ISHMAN_P5PRESS 🗖





VI. CONCLUSIONS AND POSSIBLE IMPROVEMENTS

Currently the system is implemented for one beamline (3-ID) and is working very well. All of the diagnostic screens have been used for beamline hardware checkout and as an aid to software verification. The ability to monitor the entire I/O map of both chains simultaneously has been a tremendous benefit to diagnosing wiring problems and limit–switch misalignments.

A number of improvements and/or additions can be added to the system however. The interrupt driven nature of both chains is worthwhile in theory, but may not do so well in practice. There are a few signals that are periodically changing on the I/O maps which need not generate interrupts (particularly the "watchdog" signal – a pulse train traded between both chains to indicate "I'm alive" status [2]). Making special consideration for these periodically changing signals may cut down on network traffic and processor load.

At this point in time, Chain B does not pass any status information (i.e., scan times, battery condition, etc.). Although it was deemed not necessary due to the simple interlocking function of that chain [2], it will be added later to assist in debug and fault tracing.

Finally, the Alarm Handler and the Archiver have not been implemented up to this point. It would be worthwhile to log certain I/O and status points in order to reconstruct any run time faults that may occur during beamline operation.

VII. ACKNOWLEDGMENTS

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