Current Status of the Control System for the PLS 2 GeV Linac*

I. S. Ko, J. H. Kim, S. C. Kim, J. M. Kim, G. S. Lee, and W. Namkung
Pohang Accelerator Laboratory, POSTECH
Pohang 790-784, Korea

ABSTRACT

A distributed control system has been developed and successfully operated for the PLS 2-GeV linac. The system has three layers of hierarchy: operator interface computer, supervisory control computer (SCC) for data processing and device interface computer (DIC) for distributed data acquisition. The operator interface is based on a UNIX system with graphic-based development system, RTworks. The SCC consists of three subsystems: modulators, magnet power supplies and beam diagnostics. DICs attached to individual devices are placed around the 200 m long linac building. There are altogether 22 VME CPUs and various I/Os at the SCC and DIC levels. The realtime operating system is OS-9. During the preventive maintenance period in 1995, several upgrades have taken place. Beam loss monitors and beam current monitors have been added in the beam diagnostic station. We use fast sample and hold circuits to read 2 ns long pulse signals from the beam current monitors. We also report other upgrades and improvements that have been made.

I. INTRODUCTION

The Pohang Accelerator Laboratory (PAL) completed the 2 GeV synchrotron radiation source named Pohang Light Source (PLS) at the end of 1994 [1]. The design and construction work had taken seven years. The PLS consists of a 2-GeV electron linear accelerator and a 2 GeV storage ring. Currently, there are two beamlines: one for vacuum ultra-violet (VUV) applications and one for X-ray applications. From September 1995, the PLS started its service as a low-emittance light source for various research projects in material science, surface physics, biology and semiconductor applications using X-ray lithography.

The 2 GeV linac has 11 klystrons and modulators ion the ground floor and 42 accelerator sections in the tunnel. The overall length is 150 m and the average accelerating gradient is 15 ~ 20 MV/m. In order to achieve such a high accelerating gradient, 80-MW klystrons and SLAC-type RF pulse compressor systems (SLED) are used. There are also many magnet power supplies, vacuum monitors and various beam diagnostics devices. The circumference of the storage ring is 280.56 m. The storage ring lattice is based on the triplet-bend-achromat (TBA) with a 12-fold symmetry. There are 36 bending magnets, 144 quadrupoles and 48 sextupoles. There are three re-entrant type RF cavities with a 60 kW klystron for each. In order to correct the beam orbit, there are 108 beam position monitors and corrector magnets around the storage ring. There is a 96-m long beam transport line (BTL) to connect the linac and the storage ring.

Even though the control systems of the linac and the storage ring were developed by different teams, there are three common factors. Each system has a three-level hierarchy structure and a VME-based system with OS-9 operating system. and all custom-made codes are written in C.

The linac control system includes the main linac and the whole BTL except the Lambertson DC septum magnet which is located at the injection straight section of the storage ring. There are also two beam analyzing stations (BAS) to analyze the properties of electron beams up to 100 MeV and 2 GeV, respectively. The structure of control system shown in Fig. 1 was finalized by January 1993. At this stage, it was decided that we would use commercial products for all hardware such as CPU boards and I/O boards and concentrate our effort on developing necessary software with the help of a commercial development toolkit RTworks. Before starting the major work, we made the signal list and the design manual for the linac control system [2,3]. The actual software development started in May 1993 and the initial phase of the control system was completed by the end of June 1994. It played an important role during the commissioning of the 2 GeV linac, which started at the beginning of January 1994.

At present, the linac control system provides reliable service for daily operations. However it is continuously being upgraded, based on operational experiences and diagnostic equipment added.

II. HIERARCHY OF LINAC CONTROL SYSTEM

* Work supported by Pohang Iron & Steel Co. and Ministry of Science and Technology, Korea.

Our aim for the linac control system is to provide a reliable, fast-acting, distributed real-time system. As shown in Fig. 1, there are three layers in the control hierarchy; operator interface layer, data process layer and data acquisition layer. The last two layers are based on the VME realtime system. There are also three subsystems with diferent functional characteristics: modulators and the microwave system (MK), magnet power supplies (MG) and beam diagnostics (BM). Several special systems are connected directly to the data process layer. These various elements are linked by four independent ethernets.

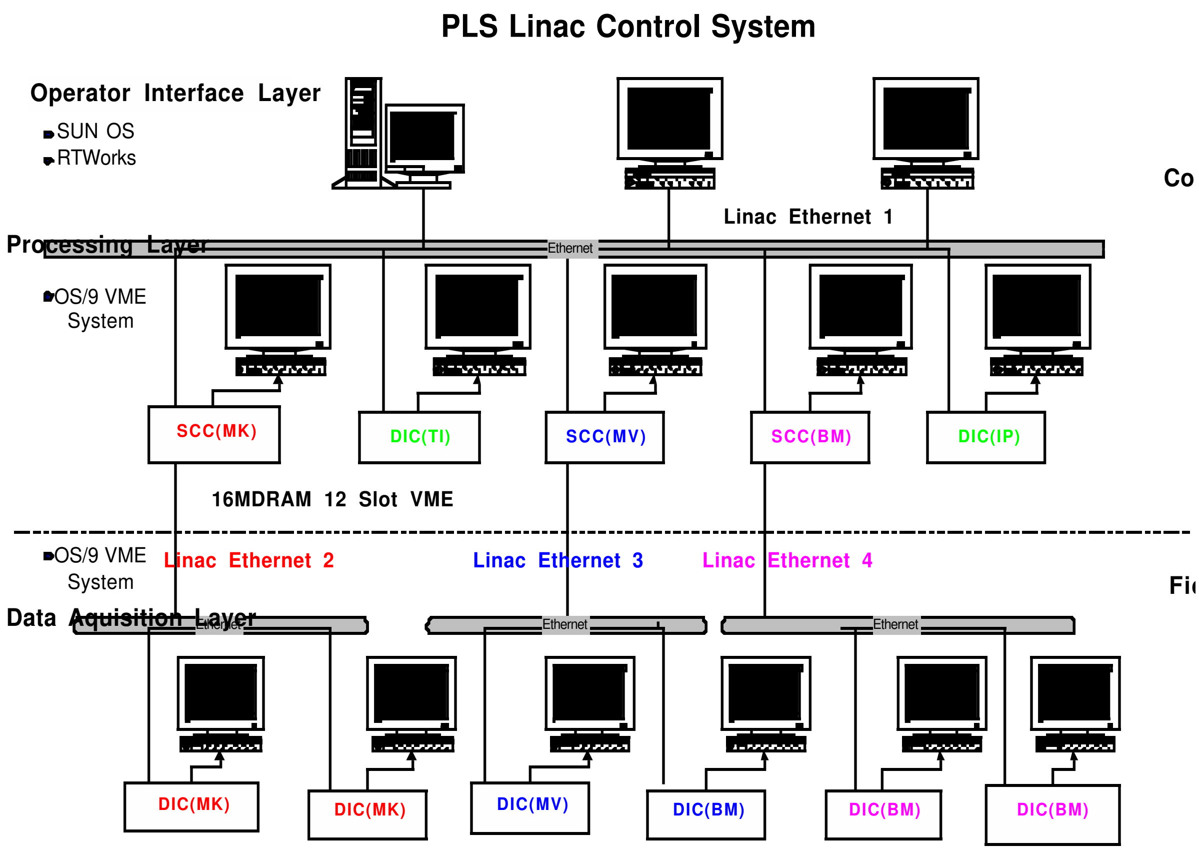

Fig. 1: Hardware structure of the PLS linac control system

A. Device Interface Computer (DIC)

This layer is directly connected to the individual devices to be connected or monitored. The local computer connected to the individual devices is called the device interface computer. Each DIC is consisted of an ELTEC E-16 CPU board, a 14” EGA graphic monitor, a draw-type keyboard, and several I/O boards mounted on the standard 19” rack. The E-16 board includes a Motolora 68030 CPU, 4 MB of DRAM (MDRAM), an EGA compatible video port and an ethernet port. There is an extra memory board with 4 MDRAM in each DIC. The operating system is OS-9 with the MGR graphic development tool. On-demand local computer control is available to all DICs. This feature is extremely useful for the local commissioning and testing of an individual device, especially the 200 MW modulators.

There are eleven units for the modulator and microwave control systems (MK) and three units for magnet power supplies (MG). There are also two units for beam profile monitors and other diagnostic equipment in the linac and the BTL. All DICs are located in the klystron gallery.

All of the I/O boards used in the VME system are commercially available. Table 1 shows a summary of these I/Os currently used in the linac control system.

Table 1: Summary of I/O boards

Name	Functions	No *	Station
TSVME400	48 digital input (optically isolated)	13	MK, BM
TSVME401	32 relay-output	13	MK, BM
TSVME410	Multifuction	11	MK
TSVME500	4 x RS422	11	MG, Buncher
TSVME208	4 MDRAM (memory)	15	MK, MG, BM
AVME9470	80 I/O channels	10	MK (IPA)
AVME335	Image Processing	1	IP
E-16 GPIB	GPIB port	11	MK (oscilloscope)

(* Number of used I/Os as of September 1, 1995)

B. Supervisory Control Computer (SCC)

In order to avoid a heavy workload on the main computer, we divided the linac control system into the three functional subsystems noted above. The role of the SCCs is to act as an intermediate data manager for the assigned subsystem.

Each SCC unit consists of an ELTEC E-7 CPU board, a 19” monitor located on the sub-control console, a 3.5” floppy disk and a 900 MB hard disk. The E-7 board has a Motolora 68040 CPU, 16 MDRAM and a workstation graphic board. There are two ethernet ports in each SCC; one for the data acquisition layer and one for the operator interface layer. Some units are equipped with a streaming tape backup system. All SCCs are installed in one standard 19” rack in the sub-control room which is situated next to the main control room, only separated by large glass windows.

Three more such units are installed in another standard rack in the same room. Their major role is to alow the development of system software without disturbing the main control system; they can also provide backup functions for the main SCCs in case of troubles.

C. Operator Interface Computer (OIC)

This is the main computer for the PLS linac control system. The OICs are actually a SUN-4 sparcstation and two X-terminals connected to this SUN workstation. They are located on the main console. There is one more system in the sub-control room, namely the backup system. The OS is UNIX, and RTworks is intensively used to optimize graphics and data handling between the UNIX system and the OS-9 system.

There is one more SUN-4 workstation in the main control room for physics-related work. The accelerator physicists can develop various simulation codes and apply the results to operations after development.

III. SOFTWARE

In parallel with the hardware structure, we use three layers in the software structure. Subsystems such as MK, MG, and BM are monitored and controlled by individual tasks running on the appropriate layers as shown in Fig. 2. There are two important features in the linac control software; the client/server routines to exchange data and commands between layers and the separation of monitor/control tasks. When the operator selects a command from an appropriate window, it sends it down to the designated device via control client/server routines in the realtime system. The data collected by a given command returns to the operator’s window through a separate route. The communication between layers is made using the TCP/IP protocol.

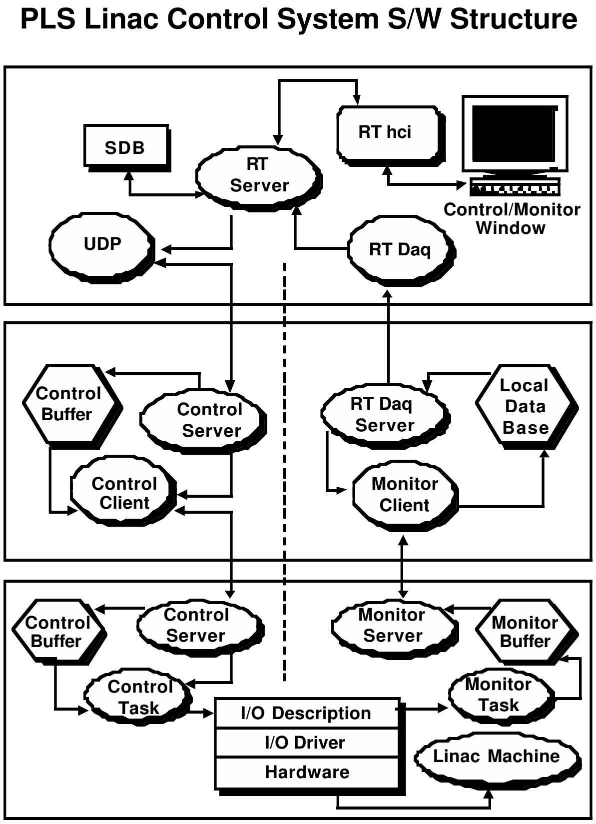

Fig. 2: Software structure of the PLS linac control system

A. Data Acquisition Layer

The major roles of the data acquisition task in the DICs are as follows; to store monitored data from individual devices to the designated buffer (m_buffer) regularly and to send updated data to the SCC upon request. On receiving a control command from the SCC, the corresponding control task sends data or messages to control individual devices in realtime through the appropriate I/O ports. Other important roles of the data acquisition task are to monitor any malfunction of the connected devices and to provide emergency cures if possible as well as to report the status to the SCC.

B. Data Processing Layer

The major role of the data process task is to collect the updated data from the attached DICs and to store them in the realtime database. These data are sent to the RTdaq running on the OIC upon requests made by the operator. Also a corresponding task sends control commands to the appropriate DIC in real time. All the required application software is running in real time in this layer including client/server routines for the ethernet communications. Every piece of data in the linac operation is stored in the RAM area temporarily and transferred to the disk for permanent record.

C. Operator Interface Layer

A commercial software package named RTworks is being used to develop graphic-based operator interfaces. RTworks is actually an integrated development toolkit for data handling between client/server systems. Using this toolkit, it was possible for one software engineer to develop all the operator interfaces required for linac control in a year.

The data received in the RTdaq from realtime CPUs are sent to the RTserver by inter-processor communications and they are displayed in the monitor windows by the RThci routine. A command selected by a mouse action is sent to the SCC through user-defined processes.

There are several windows for operators to control and monitor individual system such as microwave, bunchers, IPAs (isolator, phase shifter and attenuator systems to provide the best microwave conditions for the klystrons) and modulators. Each window has a value display area and a control sub-window. All the control actions can be made by selecting areas with a mouse or selecting items from pull-down menus. Figs. 3 shows the main window for the linac control system. This window includes the status of 11 modulators and phase angles for IPAs. Subsystems such as magnet control and monitoring windows can be started by selecting appropriate commands from the pull-down menu.

IV. UPGRADE PLAN

As of the end of June 1994, most of the linac control system was completed. It was used for the commissioning to obtain 2 GeV beams and for the routine operations to provide beams to the storage ring [4]. Since then, only minor debugging work has been necessary. However, there are several things to be added to the present control system. Signals from beam current monitors (BCM) and beam loss monitors (BLM) will be displayed in the main control window. This work involves fast signal processing due to the 1 ns pulse duration of the electron beam. At present the necessary electronics, including fast sample/hold circuits for the BCM are completed. Full tests of the BCM and BLM electronics and data acquisition routines will be made in the next preventive maintenance period which is scheduled for summer 1996.

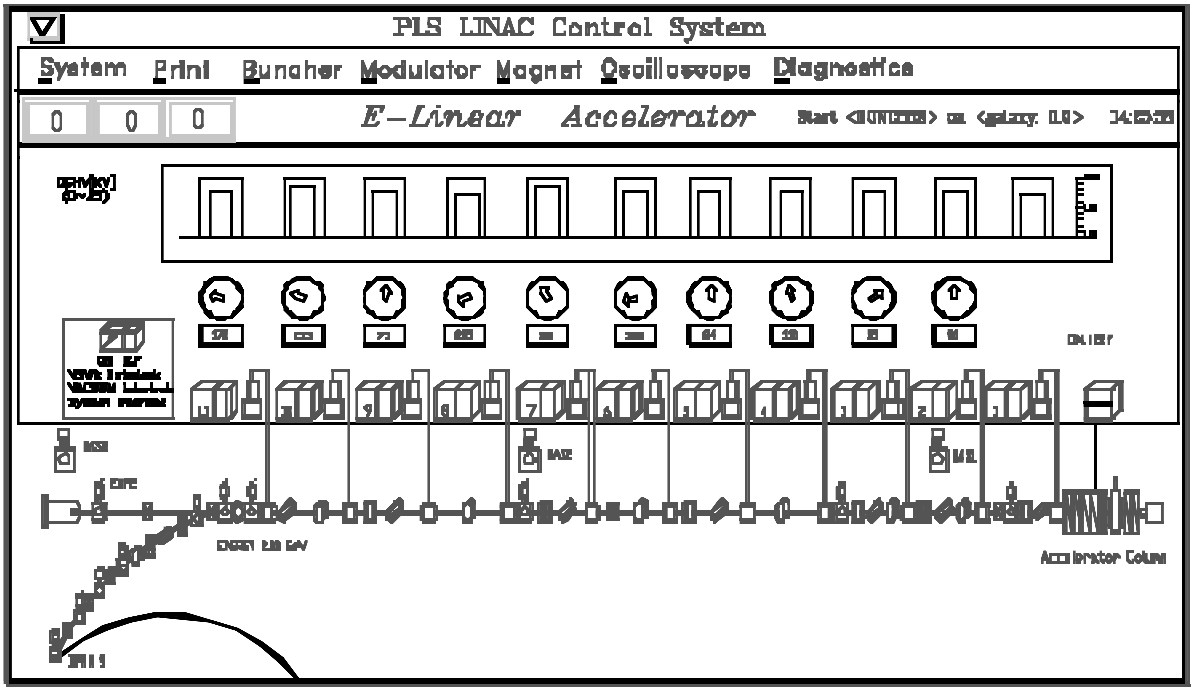

Fig. 3: Main window for the PLS linac control system

The timing system will be incorporated in the main control system after completing optical communication circuits between the individual time delay units located in the sub-control room and the corresponding modulators in the klystron gallery. There will also be a new electron gun control system.

V. ACKNOWLEDGMENTS

Our grateful thanks to the team of linac operators, especially to M. K. Kim, K. W. Kim, N. S. Sung, H. S. Kang, and S. W. Kang for their valuable help and suggestions in developing the linac control system.

VI. REFERENCES

1. "Design Report of Pohang Light Source (revised ed.)," Pohang Accelerator Laboratory, 1992.
2. I. S. Ko and W. Namkung, "Signal List for 2-GeV Linac," MA/LN-93001, Pohang Accelerator Laboratory, 1993.
3. I. S. Ko et. al., "Design Manual for PLS Linac Control System," MA/LN-93002, Pohang Accelerator Laboratory, 1993.
4. W. Namkung et. al., "Operation of PLS 2-GeV Linac," in Proc. of 1995 Particle Accelerator Conference, Dallas, Texas, USA, May 1995 (to be published).