STAR Controls System

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Abstract

The Slow Controls System for the Solenoidal Tracker At RHIC (STAR) is presented. The application of the Experimental Physics and Industrial Control System (EPICS) to this system is discussed. A prototype Hardware Controls system incorporating the High-level Data Link Control (HDLC) protocol has been developed and tested. This Controls system is used to provide a number of on-chamber control functions as well as an alternative path for accessing digitized detector data. Results from the preliminary system tests are presented.

I. The STAR Experiment

The STAR detector is located on the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory. The STAR experiment will investigate collisions between gold ions accelerated to 100 GeV per nucleon, searching for evidence of the transition of nuclear matter to a quark-gluon plasma state [1]. The use of a Time Projection Chamber (TPC) will enable the STAR experiment to track thousands of particles per event as well as examine and correlate individual particle properties and global event variables. The STAR experiment will be on-line in early 1999.

II. STAR Controls System

The main purpose of the STAR Controls System is to ensure the validity and consistency of the recorded data so that physics data may be extracted. To accomplish this the STAR Controls System:

- Sets the system parameters according to a pre-defined sequence
- Saves and restores the detector configuration
- Provides an alternate data acquisition path
- Verifies correct functioning of the detector by monitoring the subsystem parameters
- Warns about possible subsystem malfunctions
- Handles alarms
- Controls normal operations
- Provides fault diagnostics
- Allows for simultaneous testing of different subsystems
- Archives information about the subsystem parameters in an easily accessible way
- Provides logging capability

EPICS was selected as the foundation for the STAR Controls software environment because it incorporates all of the system features outlined above. EPICS was designed by Los Alamos National Laboratory and the Advanced Photon Source at Argonne National Laboratory. At STAR, EPICS is run on a UNIX-based workstation connected to VME crates operating under VxWorks, a real-time operating system [2].

EPICS was designed as a development toolkit and common run-time environment that allows users to build and execute real-time control and data acquisition systems for experimental facilities [3]. A principal component of EPICS is its database. The database is an ASCII file that is configured off-line using a Database Configuration Tool and is loaded into the memory of an Input Output Controller (IOC). The database consists of specific records written for alarm checking and setting and for monitoring and controlling parameters within each subsystem.

The current STAR operator interfaces (OPI) are SUN IPX workstations. A display editor is used to create and modify the OPI displays. This allows the user to design the specific control needed for the application [3].

The system hardware consists of a VME crate for each subsystem using commercially available industrial interfaces and programmable controllers wherever possible. The monitoring tasks and system control are distributed on SUN IPX workstations. The workstations and VME crates are networked with ethernet. If a single input-output-controller (IOC) becomes saturated, the processing can be shared with other IOCs. If an operator interface were to become saturated, then the processing could be distributed to other OPIs [2]. The organization of EPICS is shown in figure 1.

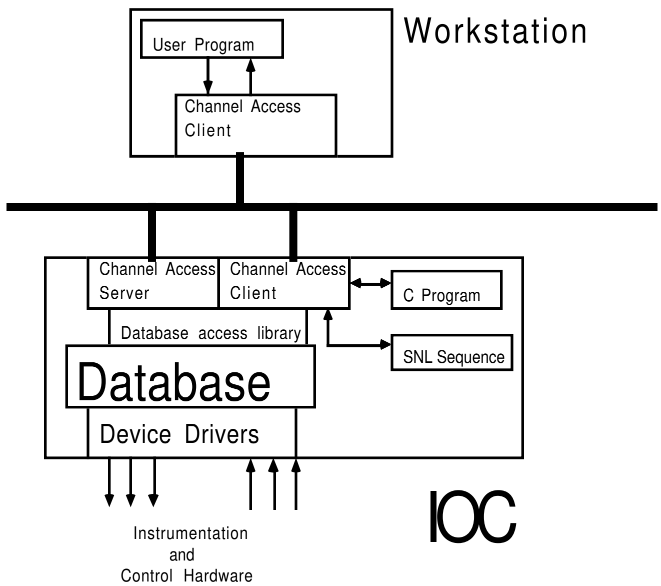

Fig. 1. Configuration of EPICS.

Each subsystem in STAR has an EPICS-based hardware control system which is used by Experiment Control as a tool to control and monitor the performance of the detector hardware. Experiment Control does not execute detailed control of subsystem hardware directly; it issues commands to the appropriate subsystem control processes. This method of implementation serves two purposes. First, it preserves the "chain of command" so that it is clear who or what is controlling a piece of hardware. Second, it provides an interface between the experimentalists working on subsystem control and those involved in Experiment Control.

III. System test of the Slow Controls Interface with the TPC

The STAR TPC readout boards require a link to the Slow Controls system for a number of testing, control and monitoring tasks as well as to provide STAR with an alternate data acquisition path. Since each readout board stores over one megabyte of data per event, the Slow Controls link speed is required to be in excess of 10 kB/s to be of use as an alternate data acquisition path. This link must operate well from the electronics platform to the TPC endcaps, a distance of 30 meters, as well as in the 5-kG magnetic field present in STAR. Due to space considerations, the link must also accommodate a multi-drop topology to reduce cabling [4],[5]. To accomplish this, a bi-directional data transmission and control system that interfaces easily with the EPICS software environment, is required.

HDLC was selected as the protocol for the TPC/Slow Controls link because it incorporates all the requirements outlined above. The link throughput is about 70 kB/s. In the STAR implementation, the signals are sent using RS-485 drivers and receivers. The differential transmission is important to avoid ground loops. The major disadvantage of the generic HDLC is that it requires some software development and more on-board hardware than some of the more highly integrated choices [4],[5]. The HDLC interface accepts function-specific parameters passed from an EPICS database to execute a desired data transmission.

The Slow Controls TPC System test was designed to test the TPC readout boards functionality as well as the Slow Controls and Data Acquisition links that interface with each readout board. The TPC Front End Electronics (FEE) boards receive event signals from the chamber, then perform amplification and digitization of the signals. The TPC readout boards receive input from the FEE boards and store the data in event memory or send the information to the Data Acquisition (DAQ) subsystem through a fiber optic link. By pulsing the FEE boards with known signals the Slow Controls link is used to verify that the signals were properly amplified, digitized and stored in memory. The Slow Controls link is also used to write random data to the readout board memory. This data can be read from the readout board by DAQ and also by Slow Controls. Comparisons can be made between the original data and the data sets that are read by DAQ and Slow Controls. This method is used to test data transmission on the fiber optic link as well as on the Slow Controls link.

The TPC has two endcaps each of which is divided up into 12 super sectors. Each super sector network is made up of 6 readout board slave nodes and one commercially-built master node in a VME crate. The slave nodes are based on a 68302 microcontroller running at 20 MHz and are built on a 73-mm by 84-mm printed circuit "daughter" board which is designed to plug on to a readout board. The board requires +5 V at 200 mA, and communicates with the readout board via memory mapping [4]. The commercially-built master node is a Radstone SBCC-1 which is based on a 68360 processor and supports 4 HDLC channels. For the system test, one TPC sector was fitted with readout boards and slave nodes which were then connected to one HDLC channel on a Radstone master node. Timing signals were sent from the Radstone board and reflected back by the readout boards to generate a proper phase read clock. This was done because the 68302 serial ports cannot self clock. The hardware configuration for the system test is shown in figure 2.

The HDLC-EPICS interface consists of subroutines which are loaded into the IOC at boot time and perform read and write transactions to and from a TPC readout board memory in a transparent manner via the Radstone board. The HDLC command format allows specification of starting address, network number, slave node number, number of 16-bit words to read or write and an offset value which is the number of 16-bit words to skip between each read or write. Commands sent via the HDLC link may read or write up to 1012 16-bit words [4],[5].

A new EPICS software record was created that allows EPICS-based control programs to pass the appropriate parameters to the HDLC interface on the Slow Controls side. This record was based on a similar record for VME data transfers developed at the University of Chicago Synchrotron Radiation Community. The record allows the user to select which network and node to access and to input a starting address, the number of words to read or write and an offset value.

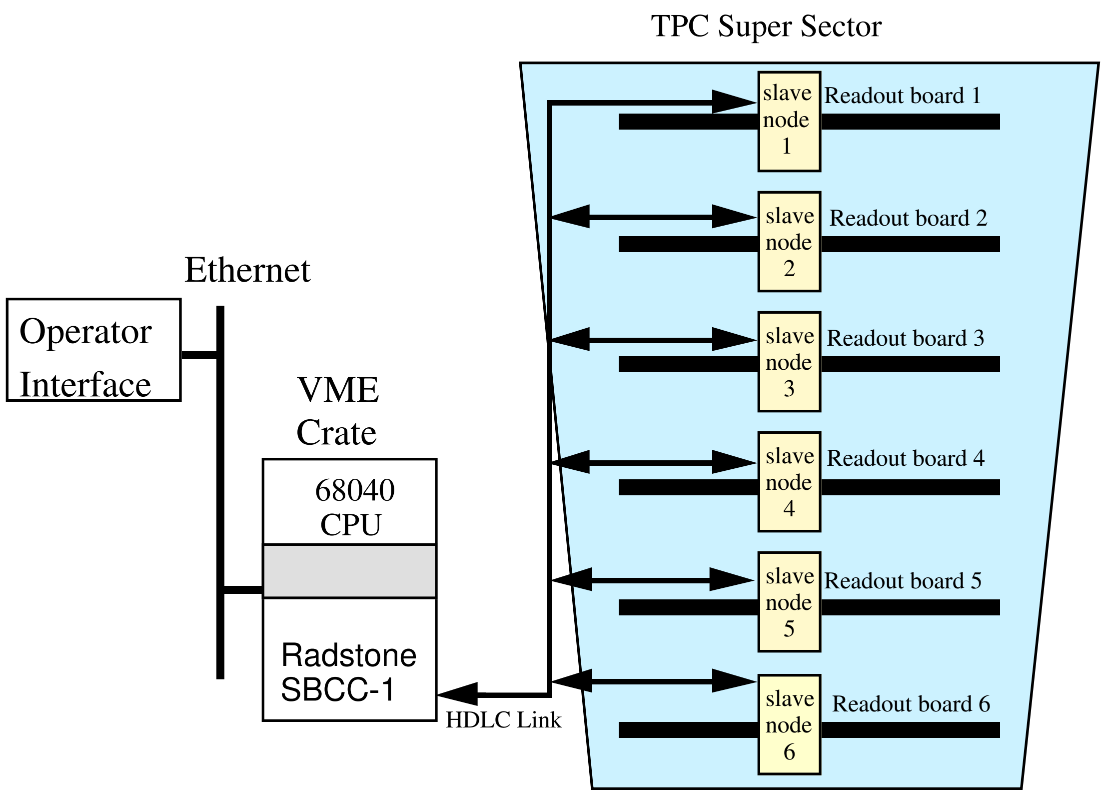

Fig. 2 Hardware configuration for system test. There are six readout boards per super sector, each of which is slave-node daisy-chained by an HDLC cable to a Radstone board. (Each Radstone board can service up to 4 HDLC links, only one is shown.)

IV. Summary

A solid foundation has been laid for interfacing the EPICS-based STAR Slow Controls system with the STAR TPC subsystem using the HDLC protocol. Preliminary results show that the HDLC-EPICS interface is capable of reading and writing event data to and from the TPC readout boards reliably. Applications have been built that control and monitor functions on the readout board. The transfer of randomly generated event data from a ASCII file on a workstation to the memory of a 68302 daughter board and back for comparison has verified the proper functioning of the HDLC link.

VI. References

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