Microcontrollers applications for IHEP accelerator control.

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1. Introduction

About 14 years ago Intel introduced the MCS 51 family of 8-bit microcontrollers. They are still on the market, keeping compatibility with their successors, which have expanded in functionality and improved in speed. This family is suitable for use in the most popular embedded control applications. The last members of the MCS 51 family provide very high performance and superior code density.

Dallas Semiconductor designed a few 80C32-compatible chips based on the Dallas High Speed core. As a result, every 8051 instruction is executed between 1.5 and 3 times faster than the original one for the same clock rate. The DS80C520 is the fastest of them. It offers a maximum clock rate of 33 MHz, yielding a single-cycle instruction execution time of 121 ns (8.25 MIPs).

As was mentioned above, the 8-bit 8051 micro is now 14 years old, and characteristic of many teenagers, is expected to experience a quick surge in growth. Two 16-bit derivatives soon will be widely available. The 3-stage CPU architecture of the new MCS 251 microcontrollers (Intel) boosts 8-bit performance five times by just swapping chips and up to 15 times by incorporating new instructions and addressing modes. Philips Semiconductors has announced the sampling of the XA-G3 microcontroller, the first member of Philips' extended architecture family. The G3 is a powerful, general-purpose microcontroller that is code compatible with the 80C51. With a 30 MHz clock, the XA-G3 has a typical instruction execution time of 100 ns.

It is very important that all mentioned microcontrollers are fully code- and pin- compatible with the MCS 51 microcontroller family, so one can increase significantly performance without reworking the old design. On the other hand the speed and efficiency of these micros allow easy handling of a broad range of highly-demanding embedded requirements in the control, timing and computation functions.

2. Field-bus controller VBC

The field-bus controller VBC designed in IHEP is a typical example of latest generation microcontroller applications for accelerator control. The VBC supports the MIL-1553-STD-B communication, which has been extended in CERN to meet the specific requirements of accelerator control. The VBC is a one-board VME module based on the 8-bit microcontroller DS80C320 from Dallas Semiconductor. The VBC simulates all functions of the NBC [1] and may replace the latter without any hardware or software adjustments.

The DS80C320 micro is pin-compatible with the standard 80C32 and offers the same timer/counters, serial port, and I/O ports. The DS80C320 provides several extras in addition to greater speed. These include a second full hardware port, seven additional interrupts, programmable watchdog timer, dual data pointers, power-fail interrupt and reset. The DS80C320 is extremely familiar to 8051 users but with a maximum clock rate of 25 Mhz provides the speed of a 16-bit processor.

The VBC micro makes a link between the 1553 bus protocol and data exchange with the VME CPU. These data pass through a 16 Kb dual port memory (DPM) and are synchronized with an interrupt to the host computer. A control and status register (CSR), accessed either from the host CPU or the microcontroller, allows to identify each interrupt. The DS80C320 performs three real-time tasks: receive/transmit, slow polling and fast polling [2]. It allows the avoidance of wasting host CPU time. The fast serial communication (1Mb/s) is performed under full control of the microcontroller.

Although the NBC is based on a conventional 16-bit microprocessor, the performance measurements show similar timing responses for the VBC and NBC, which are mostly defined by the serial protocol itself. Nevertheless this experience has shown that high grade 8-bit micros may force out 16-bit microprocessors today in many control applications, providing simplicity of design, low cost and high performance.

The high speed microcontrollers can replace conventional logic-based state machines. This idea has been implemented in the development of different I/O modules for U-70 controls.

3. General structure of microcontroller-based modules

The general structure of microcontroller-based VME modules consists of a DPM, a CSR, an MCS 51 family microcontroller and application dependent peripherals. All modules provide some logical compatibility; that means a uniform scheme of register field and DPM allocation within a module's address space, plus a mandatory defined format for the device control and status register (CSR).

Each module allocates the 32 Kb of VME address space that are shared between the module's register field (the lowest 256 bytes) and the DPM. The dual port memory is divided into 4 areas: the Command Area, the Reading Buffer, the Polling Area and the Error Buffer.

The Command Area is used by the host to write a sequence of actions (commands) followed by data. Tables of vectors for function generators, scan-lists for multichannel ADCs and settings for timers are placed in this area.

The Reading Buffer contains some data captured by the microcontroller during command execution and prepared for the host. They are the results of analog to digital conversions, contents of counters or any data requested by the host.

The Polling Area is a special command area that is filled by the host if a microcontroller performs periodic input signals polling and then compares results with some predefined conditions placed in the same area. The polling is a typical control task for modules having a number of analog or digital input channels.

The Error Buffer is used by a microcontroller to report about any faults that occur during command area execution.

These areas have different sizes in different I/O modules but accesses to each of these areas are performed under software control using the same CSR flags.

4. Module register assignment

Within the module's registers, the lowest 8 are reserved for functions that apply to the whole module. These are: the Interrupt Vector Register (IVR), the Control and Status Register (CSR), the Module Reset Register (MRR) and the Module Identification Register (MIR).

The 16-bit IVR allows the assignment of the module interrupt to one of seven interrupt levels and to program the vector number, supplied with the interrupt acknowledge VME cycle. This register could only be accessed from the VME side in read or write mode.

A host writing action in the MRR results in a complete reset of the module including the microcontroller.

The 16-bit read-only MIR contains very useful information for the host: crate number(C), module number(M), and identification number(I) -- the unique bit pattern assigned to each type of modules.

The CSR is a dual port register accessed either from the VME bus or the internal microcontroller bus. It is used to synchronize the data exchange through the DPM between host and microcontroller. The content of the CSR reflects the DPM organization. Setting POLL by the host CPU starts the polling action. Detecting any changes by microcontroller activates the CHG flag together with INT. Setting GO by the host causes the microcontroller to execute the sequence of actions written in the Command Area. The ERR flag shows that the Error Buffer is filled with information concerned the last detected fault. The active DFH (Data for Host) flag means that data in the Reading Buffer is ready for the host.

The host sets two additional flags INE (Interrupt Enable) and TST (Test), enabling a VME interrupt or activating an internal test. The microcontroller status is shown by HALT and module status by RDY.

Other bits of the CSR are reserved for future assignment.

5. Technical parameters of the microcontroller based I/O modules

The logical compatibility of I/O modules leads to the standard hardware implementation of the essential part of the module, including VME interface, DPM, CSR and microcontroller with support. This provides the facility whereby I/O functional modules covering a different range of tasks may be largely developed around a common structure, with the resulting benefits in development time, documentation, training overheads, etc.

The set of VME microcontroller-based I/O modules includes the scanning ADC (VSA), the two-channel function-generator (VFG) and the timing generator (VTG). In the following are some technical parameters of these modules emphasizing the microcontroller application.

The VSA is the 12-bit, +/- 10V, 16-channel differential/32 single-ended ADC with 24 Kb of data store buffer. Everything from the selection of sequences of channel sampling, sampling rate and operating mode, to the size of data stored are software programmable. The high speed microcontroller DS80C320 allows a maximum sampling rate of 5µs/channel.

The VFG is a 16-bit, +/- 10V, two-channel function-generator intended for power supply control. The 8-bit DS80C320 provides a maximum rate of 50 µs/point, as has been requested for this application. The microcontroller spends most of this time computing the next point. An estimation shows that a compatible microcontroller with 16-bit internal structure, such as Intel's 80C251SB, can significantly improve the maximum rate up to 10 µs/point using the same algorithm.

The VTG is a timing counter board providing the user with 8 general purpose, 16-bit timer/counters with a maximum rate of 4 MHz and 16 channels with 1 ms resolution and 1 µs accuracy. Each counter is fully programmable from a user-defined start value up to that selected from one of the range of sources. The contents of each counter may be read and stored at any time without disturbing the counting process. The board can also work as an 8-channel pulse-width modulator (PWM) or in a combination of PWM and timing channels. The 8-bit DS80C320 simulates the 16 slow channels in software, simplifies the setting of the fast channels and controls the PWM outputs. This module may generate, in one of the applications, a setting value (PWM output) and two timing pulses for 8 power supplies.

Conclusion

The microcontrollers of the last generation can be successfully used for the development of high performance VME modules as has been shown here. The present approach gives to designers some advantages, the most important of which are:

1. Much of the hardware development portion of the project may be reduced to the design only of function-dependent parts. This obviously results in big savings of development time and money and reduced technical risk.
2. More of the development budget is applied to product-specific software development.
3. The same basic product design could be fitted with different types of compatible microcontrollers allowing faster product operation with similar features or enhancing features while maintaining acceptable performance.

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References

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[2] C.Pignard, G.Surback, NBC, CERN SL Note 93-92 (CO).