HIGH PERFORMANCE DSP DATA ACQUISITION ENGINE FOR ACCELERATOR INSTRUMENTATION AND CONTROL

K. Woodbury, J. Smolucha, C. McClure, K. Fullett, B. Chase
Fermi National Accelerator Laboratory*
Batavia, Illinois 60510 USA

ABSTRACT

A low cost, high performance data acquisition and processing module is being developed incorporating the Super Harvard Architecture Computer (SHARC) DSP made by Analog Devices. The module provides independent ADC channels and high-speed, real-time data processing with pre- and post-trigger data collection. Using these modules, both the processing capabilities and number of ADC channels in the Fermilab Tevatron and Main Ring accelerator systems will be expanded. There are also potential applications in other accelerator instrumentation and control projects.

1. INTRODUCTION

The current Main Ring and Tevatron Accelerator Data Acquisition Systems provide over 3,000 multiplexed analog-to-digital conversion channels. The hardware used for this data collection network consists of 64-channel, multiplexed analog-to-digital conversion chassis, MADC-I (12 bit) and MADC-II (14 bit) [1],[2]. A CAMAC module [3] with embedded micro-processor is used to manage data collection, timing and data transfer to the ACNET control system [4].

This extensive network of channels provides a very effective mechanism for monitoring at both high and low frequencies. Low frequency monitoring (15Hz) can be provided essentially for all channels simultaneously. Higher frequency monitoring (66 - 100 KHz for MADC systems) can only be provided for one channel at a time. If multiple channels of high speed data collection are required this sampling rate must be divided between the desired channels.

The physics and accelerator operations staff expressed the need for more high frequency data collection channels in a single location and expanded capabilities for pre- and post-trigger data collection. In addition, continuous data processing such as FFTs and digital filtering was also desired.

Addressing these needs an R&D effort was started to design a new data acquisition system which could provide these added capabilities and complement the existing MADC system. This new system has been named the Data Acquisition System, version one (DAS I).

2. THE DAS SYSTEM

The essential components of this planned VMEbus-based system are shown in figure 1. All modules are 6U x 160 mm.

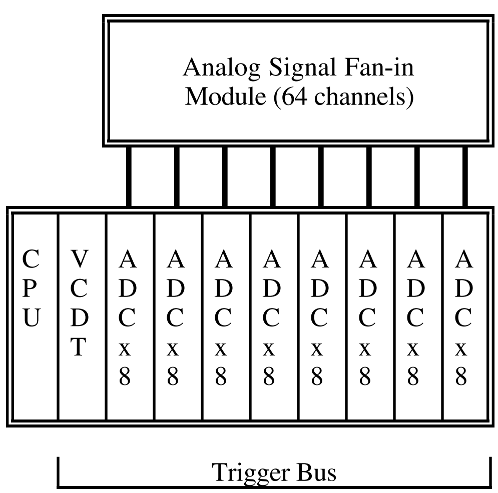

Figure 1. DAS VMEbus Chassis and Fan-in Module

* Work supported by the U.S. Department of Energy, contract No. DE-AC02-76CH03000.

- *VMEbus crate.* This VMEbus chassis is specifically designed with a low switching noise power supply and 6U x 160 mm transition modules in the rear. These modules provide connections to the Analog Fan-In Box (shown above), and the capability of bussing between P2 connectors.

- *VMEbus Clock Decoder and Timer (VCDT).* This module is a modified VMEbus Universal Clock Decoder (VUCD), which provides eight channels of delay timers combined with an interface with accelerator timing systems. For a more detailed description of the VUCD module see references [5],[6].

- *Trigger Bus.* This trigger bus provides a connection from the VCDT to all of the ADC converter boards, synchronizing data collection with the accelerator timing. This provides an equivalent connectivity to that provided by VXIbus TTL trigger bus specification. This can be implemented using the rear transition modules.

- *CPU / System Processor.* The current system processor of choice is a Motorola MVME162 - 68040 based processor running the VxWorks operating system. This processor has an on-board Ethernet adapter providing a network connection to the control system.

- *ADC module (under development).* Each of these ADC modules will have an on-board DSP and eight independent input channels with a minimum effective resolution of 14 bits. The planned conversion rate is 1-2 MHz. This frequency range was chosen as 640 kHz would be the minimum frequency to provide turn-by-turn data collection in our Booster and Anti-proton Source accelerators. Differential input is desirable but pre-trimmed differential amplifiers have not been found with the 10-20 MHz input bandwidths desired for this application. Anti-aliasing filters are also desired.

- *Analog Fan-in Module (under development).* This external chassis will allow for numerous user inputs which are then cabled to the J2 analog inputs.

The architecture of the DAS ADC module is described below.

3. DAS ADC ARCHITECTURE

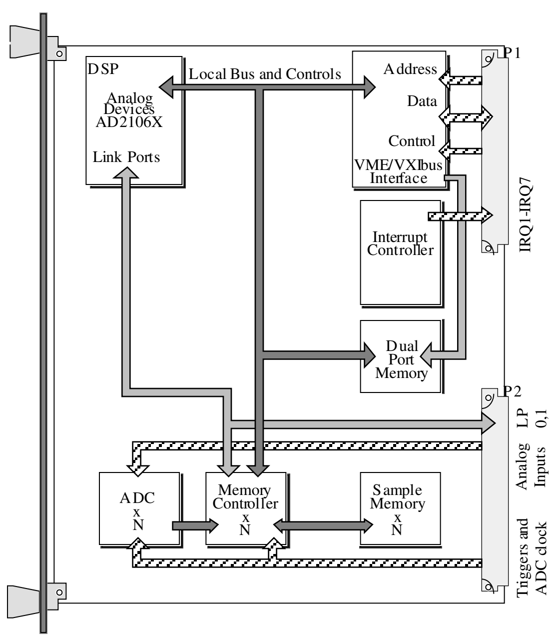

Figure 2. Simplified DAS ADC Block Diagram

The main components of the DAS ADC board are the following:

- Digital Signal Processor (DSP)
- Memory Controller and Sample Memory
- ADC Converters and Signal Conditioning
- VME/VXIbus Interface
- Event Trigger Inputs
- Dual-Port Memory

3.1 Digital Signal Processor

The primary use of the DSP is for real time data processing. Examples include gain and offset compensation, digital filtering and FFT computation. Additional functions provided by the DSP include controlling DMA transfers over the VME/VXIbus backplane and providing on-board process control as well. The DSP that was chosen is the Super Harvard Architecture Computer (SHARC) DSP developed by Analog Devices.

The SHARC DSP has a number of unique features. It has a maximum processing rate of 40 MIPS and 2-4 Mbits of internal program and data SRAM. The DSP was developed for high-speed radar data processing and was specifically designed to operate in a mesh architecture, where each processor can have a dedicated high speed communication link (Link Port) with up to six other processors. The Link Ports connect directly to an internal DMA controller as well. These Link Ports are one of the features which make the SHARC DSP well suited for the DAS ADC as described below.

3.1.1 Real Time Data Transfers

Real time data transfer to the DSP can be done using the Link Ports. These Ports can be used to transfer four bits of data at twice the clock rate of the DSP processor. This translates to 33 or 40 Megabytes per second depending on the speed of the processor. These Link Ports were originally designed for high speed processor-to-processor data transfer, but for our application they are ideal for real time data transfer from the ADC converter. Data transferred to the Link Ports feed directly through to the on-chip DMA controller which can be programmed to interrupt the DSP when sampling is completed. This has a direct application for data acquisition tasks requiring data collection and post-processing.

It should be noted that Link Ports 2-5 will be used for transferring ADC data, and Link Ports 0 and 1 are reserved for multi-processor configurations where the ADC board is used in conjunction with another DSP module, for example, in closed loop control applications.

3.2 Memory Controller

The core of the ADC module design is the Memory Controllers. These allow for various sampling and data storage modes and thereby allows the DSP processor to be dedicated for data manipulation and processing. The Memory Controller will also contain the ADC to Link Port interface which provides the real time data transfer path described above. Both the real time data transfer path and transfer to memory can operate simultaneously.

3.2.1 Memory Controller Sampling Modes

The Memory Controller is designed with an on-board sample counter which can operate in several different modes.

- *N Sample Mode.* A pre-determined number of samples are collected and transferred to memory. The Memory Controller operates in a count down mode where the number of samples is programmed into the counter register, and sampling is terminated on under-flow of the counter.

- *Continuous Sampling Mode.* In this mode, the ADC converter is sampling and data is transferred into memory continuously. The Memory Controller operates in a circular mode where the incoming data wraps for the depth of the memory, overwriting the oldest data.

- *Gated Sampling Mode.* In this mode, ADC converter data is transferred into memory only when an input gate signal is valid.

Data collection is started or stopped using trigger inputs or by access from the DSP or host processor.

A pre-scalar counter is also provided, which allows the Memory Controller to effectively reduce the sampling frequency by an integer modulus. The pre-scalar counter is eight bits in length.

Immediate data is always available from a sample register within the Memory Controller. This is especially useful for applications where slow monitoring is required.

After sampling is complete, data is transferred through the Memory Controller to either the DSP or host processor.

3.3 ADC Converters and Signal Conditioning

The ADCs have yet to be selected, however, a converter with a minimum 14 bit effective resolution and a minimum 1-2 MHz conversion rate is desired. The maximum ADC data width in the current design is 16 bits. The maximum ADC conversion rate is determined by the speed of the Memory Controller. Simulations up to 35 MHz have been made of the Memory Controllers.

It is hoped that at least eight ADC converters will fit on each module. However, due to the small size of the module (6U x 160 mm), four channels may be all that is possible.

Signal conditioning, as described in section 2, would include differential input amplifiers and anti-aliasing filters and input voltage protection.

3.4 VME/VXIbus Interface

This module will be a D16/D32 module which is compatible with both VME and VXIbus specifications. VXIbus Configuration and Control is not required for this application.

3.5 Event Trigger Inputs

The event trigger inputs, as described in section 2, provide a mechanism for data collection to be synchronized to accelerator activity.

3.56Dual-Port Memory

The dual-port memory provides a standardized communication mechanism between the host processor and the DSP. It is used to transfer data and commands between the two processors and for issuing interrupts between them.

4. PROTOTYPE DEVELOPMENT

The current prototype development is being aimed at a high priority accelerator improvement project, the Anti-proton Source Beam Position Monitor upgrade project (PBPM) [7]. This project requires some of the exact features that can be provided by the DAS ADC board. Specifically, this project requires:

- 8 ADC channels per module.
- on-board Memory Controllers with sampling modes as described above (3.2.1) and
- on-board DSP processor.

This system does require some particular features that were not initially specified for the DAS ADC.

- *High Speed ADCs,* specifically 12 bits at a 31 MHz maximum sampling rate. This high rate is due to the super Nyquist sampling mode that is desired in this application.

- *Front Panel Analog Inputs.* Front panel analog inputs are required, as VXIbus specifications do not allow for analog signals to be fed through the P2 connector. Front panel I/O allows for a more optimized analog layout for the module.

- *Front Panel Triggering.* Front panel trigger inputs are included, in addition to the triggers provided from the VXI trigger bus (P2).

- *Front Panel Conversion Clock Input.* Front panel conversion clocks will be provided for the precise phasing of the ADCs as required by the system.

- *VXIbus Configuration Management Support.* As this module will reside in a VXIbus environment, it was preferred that the module should provide configuration management support.

  Some of these features may be incorporated into the production DAS ADC as well.

5. ADDITIONAL FEATURES

Additional features that are being considered for the production PBPM ADC board include the following:

- *Link Port Support.* Although data collection rates from the ADC are too high for full, real time data transfer to the DSP., this communication link may still be useful.

- *NVRAM for DSP Boot Memory.* The current design requires the host processor to download the DSP code at boot time. On-board NVRAM provides a mechanism to download code only when changes are needed, speeding up the system boot process. This same memory could be used for non-volatile parameter storage as well, such as channel gains and offsets.

6. CONCLUSION

The development of these modules will provide a first step towards an overall enhancement of the general data collection capabilities for the accelerator control system. In addition, high speed versions of this board will have immediate application for current VME and VXI instrumentation projects.

7. ACKNOWLEDGMENTS

Our thanks to everyone who helped us to review and develop the DAS ADC specification, including the AD/Controls Engineering Staff. And special thanks to the Anti-proton Source Beam Position Monitor Upgrade team, for helping us to develop the prototype.

8. REFERENCES

[1] K.C. Seino, "New General Purpose MADC", Controls Hardware Release no. 11.0, 1981.

[2] K.C. Seino, "Multiplexed ADC Second Generation", Controls Hardware Release no. 72.1, 1990. Fermi National Accelerator Laboratory document.

[3] J. Smedinghoff, "ACNET Fast Time Plot System", ACNET Design Notes no. 49.4, 1988. Fermi National Accelerator Laboratory document.

[4] A. Thomas, et. al., "CAMAC 190 Module Multimode Buffered MADC Controller", Controls Hardware Release no. 26.4, 1988.
Fermi National Accelerator Laboratory document.

[5] K.Woodbury and C. McClure, "Integrated Finite State Machine and RF Timing Modules for VMEbus and VXIbus Instrumentation", proceedings of the 1995 ICALEPCS conference, *these Proceedings*.

[6] C. McClure, K.Woodbury, et. al., "VMEbus Universal Clock Decoder (VUCD) User's Manual", controls hardware release, 90.01, 1994. Fermi National Accelerator Laboratory document.

[7] K. Fullet, et. al., Anti-proton Source Beam Position Monitor Upgrade Project, DOE submission for an Accelerator Improvement Project, 1995.