# Development of Fast Output VME Modules with External Clocks

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## ABSTRACT

Heavy ion acceleration in a synchrotron requires dynamic control of lattice magnets and the rf system to cover a wide variety of species and energies of ions. For example, spill-by-spill energy change is necessary for three dimesional scanning in cancer radio-therapy. The excitation pattern of lattice magnets must be switched without interruption to beam, while the rf system should follow the frequency shift caused acceleration. Since both magnet power supplies and the rf system (acceleration voltage, frequency, ferrite bias current, etc.) are driven by digital settings from VME modules, although with different clock systems, in the HIMAC synchrotron, development of a new VME module that can deal more dynamically with both magnets and rf in a unified manner is initiated as a logical extension of the present system.

Features include:

(1) 20bit (max.) pattern output with 125kHz response to external bi-directional clock triggers

(2) Versatile pattern switching with Look-Up-Table and selection command input

(3) Feed-back loop capability through VSB bus, with high performance RISC microprocessor

System construction and firmware concepts will be discussed also.

## 1. INTRODUCTION

Operation of synchrotron magnets and rf system are characterized by repetetive patterns which consist of injection, acceleration, extraction, deceleration and reset of beam. In order to accelerate the beam without losses, each field of the lattice magnets, Bending Magnets (BM) and Quadrupoles (QF/QD), should be excited in a matched strength, which is called "tracking". Power supplies of lattice magnets, accordingly, should be precisely controlled in synchronization with the thyristor trigger timing pulse. Therefore it is essential for the tracking be synchronized by means of the external clock supplied from a phase locked loop. HIMAC has already made use of Fast Digital Input/Output (FDI/FDO) modules which were developed for this purpose [1]. The rf system should also be operated in coordination with the main magnet excitation pattern, but the clock system differs from that of main magnet power supply. A bi-directional B clock of the rf system drives several patterns of frequency and voltage together with beam feed-back loops to stay with fluctuations of magnetic field for both acceleration and deceleration of beam [2]. The present control system of magnet power supplies and timing system works well. However, an advance in heavy ion therapy requires more flexible and dynamic control, as the beam delivery with pulse-to-pulse energy shift is envisaged for cancer treatment irradiation of three dimensional scanning for HIMAC and Particle Therapy Project in Hyogo prefecture [3]. A dynamic pattern operation is required to enable raster scanning, as the beam has to be swept in a Zig-zag line by controlling scanner magnets. Dynamic switching of these patterns (both magnets and rf) is demanded in various aspects of beam operations. For example, it is required to switch an arbitrary combination of magnets simultaneously during beam tuning or to use a set of excitation patterns as mentioned above. Usage is also expected to measure beam parameters, e.g. chromaticity, to initialize magnets, and to achieve digital feed-back control.

In order to select various excitation patterns of main magnets and rf system dynamically, Dynamic Pattern Input/Output (DPI/DPO) modules are now under development. This paper describes the DPO module with possible system construction.

## 2. SYSTEM CONSTRUCTION

DPI/DPO modules will be installed in subsystems where VME is used as a major equipment controller. An advanced facility such as Hyogo Prefecture's Project is expected to utilize these modules. Another example is the present HIMAC synchrotron control system. It is hierarchically structured by a network consisting of a main computer (CS) with two 20" & 14" displays, and equipment group controllers of 14 VME crates, an rf control computer (RC), a beam transport control computer and Programable Logic Controller. VME crates include timing system (TS) and Magnet Power-supply Controllers (PC), whose software is downloaded from a program server workstation (WS) [1].

The CS serves man-machine interfacing of the presentation layer. Conditions of exciting patterns of magnets etc. are set on the console displays after a decision as to the mode of operation, such as initialization of magnets, normal repetitive operation, spill-by-spill energy shift mode, adjustment of parameters or measurement of beam. These conditions will be encoded and sent to DPO as external control signals.

The TS is a system for which the main functions are distribution of base and master clocks and generation of various event signals response to CS commands. Event signals can be generated and controlled by DPO modules. Clock and event signals will then be fed to the DPI/DPOs that control magnets and rf system. DPI/DPO will be the main ingredients of PC, TS, or RC when they are constructed as VMEbus systems.

## 3. DESIGN BACKGROUND AND SPECIFICATION

The repetitive operation of lattice magnets and rf cavities in our synchrotron should be carried out independently in closed cycles in the equipment control layer, unless any commands or interrupts occur. The tracking should also be kept in synchronization with the basic clocks. Therefore DPI/DPO modules play essential parts in this layer. They should be able to communicate in real time with the host CPU of the IOC in the VMEbus system, to prepare many files of binary excitation pattern data with necessary processing on the basic data, and to respond to various external operation commands. In addition, they should have flexibility to utilize various application programs, which are downloaded from the program server on the workstation via IOC on VMEbus systems when booted.

Basic functions of DPI/DPO modules follow.

### *3-1. External clock*

DPI/DPO are supplied two kinds of basic clocksOne of these functions at 1200Hz, and supplies a trigger timing pulse for 24 phases in a 50Hz thyrister converter at the lattice magnet power supplyThe other is T-clock/B-clock which are used to control the rf system. T-clock is at a constant frequency of 50kHz while B-clock is variable up to 120kHz, in order to cover the BM excitation rate of 2.4T/sec at 0.2gauss/pulse, for both increasing and decreasing fields.

### *3-2. Pattern memory*

DPO must be able to expand the excitation pattern data from a basic trapezoid and to store the data. The necessary precision of BM data is 18 bits, while that of the rf system is 20bits, to cover an 8Mhz span in steps. To provide sufficient capacity 16MB capacity is assumed for pattern memory.

### *3-3. External control signal*

It should be able to select dynamically a required one from within several tens to hundreds of excitation patterns. For this purpose an encoded 12bit external control signal is prepared. The decoding method is effective in expanding the range of selection, although a surplus strobe signal is necessary. The module is capable of selecting not only any single excitation pattern but also a set of patterns, and to operate grouped magnets by means of masking bits, which are applied to Start or Stop events when the initialization of a group of magnets is required.

### *3-4. Look-Up-Table*

It provides a Look-Up-Table (LUT) to follow the incremental or decremental B clock of the rf system. LUT is a memory which rapidly converts any data placed on the address line to other values. This feature is useful in converting a nominal value of B clock to the rf frequency, which is not always linear with the B-field. Typically 80k table entries are required when BM is excited up to 1.6T with a B clock of 0.2gauss/tick.

*3-5. VSBbus*

VSBbus should make it possible to form a closed loop of digital feedback control by a direct connection between DPI and DPO. This feature is necessary to achieve "Iterative control" more quickly. Iterative control is effective in controlling the driving voltage of a power supply so that the current deviation can be reduced toa tolerable value by means of a digital filter. In the present HIMAC system, the host cpu module of the VME crate performs the iteration together with the FDI and FDO [4].

## 4. FEATURES OF THE DPO HARDWARE

A number of high perfomance RISC microprocessors for embedded systems have flourished in a wide range of electronic appliances. After our investigation of ability to handle external interrupts and to control timers/counters for various functions, we have made a choice of the Hitachi Super-H (SH) series CPU, which uses a 32-bit RISC core optimized for high speed and low power consumption. Another advantage of the SH-1 is that it contains several on-chip peripherals to eliminate a number of additional devices.

Table 1 shows the outline specification of DPO, for which the block diagram is shown in Fig.1. A multiple CPU system is provided on this module. The SH-1 CPU serves to control communications with VMEbus, VSBbus and all input and output ports. SH-1 also manages the SH-2 CPU, which is provided for dedicated calculation. To avoid bus contention of multiple CPUs, a separate local bus is provided for each. Pattern memory of 16MB will be used in a 3 byte/word format to cover the system requirements for rf and BM operation.

User supplied programs can be loaded into the DRAM of SH-1 or the dedicated SRAM of SH-2 and executed locally. Each CPU responds to commands and environment parameters placed in each 32kB dual-ported SRAM, is accessed from both the VMEbus and the local bus through synchronous arbitration logic.

SH-2 resides on a mezzanine board to be upgradable to an SH-3 CPU in the future. Input/output ports are also provided on the other mezzanine boards to change RS485 to TTL etc.

Table 2 shows 4 external clocks and control signals. A 12bit control signal is decoded into various ‘events’. These events are executed after the next master clock pulse except for Change signals, which are executed immediately. The LUT consists of dual 80k x 20-bit memories, of which one serves to form data output while the other receives the next input.

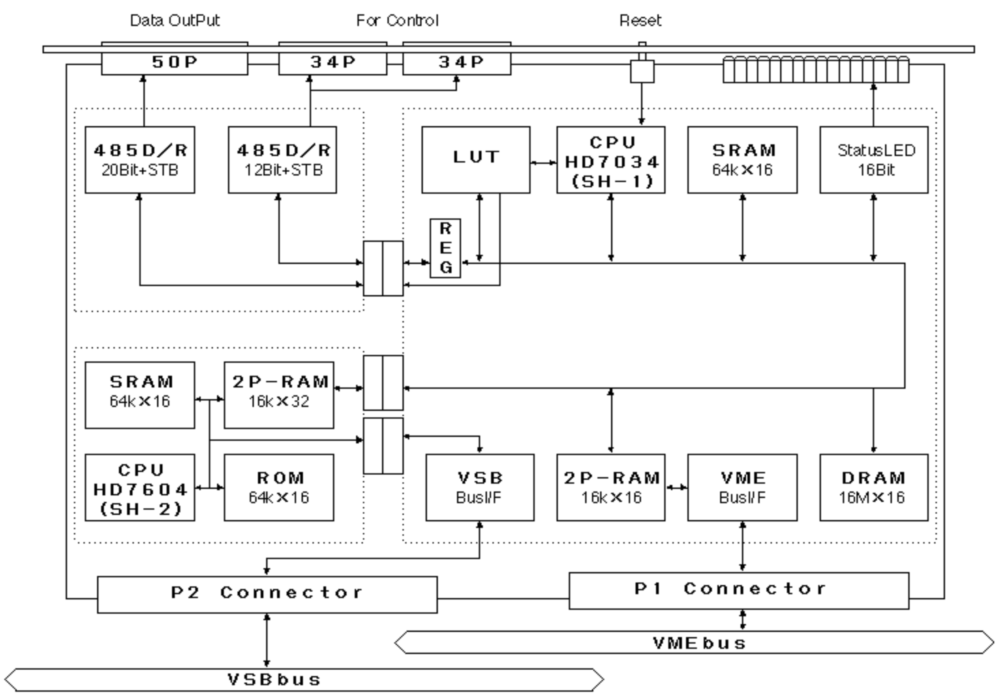


Fig1.Block Diagram of DPO

Table 1. Outline Specification of DPO

| | Main Board | Mezzanine Board for calculation | Mezzanine Board for I/O adaptation |
|---|---|---|---|
| CPU | SH7034(SH-1)<br>4kB On-chip RAM<br>64kB On-chip ROM<br>Hardware multiplier<br>9ch. Ext. interrupt handler<br>4ch. DMA controller<br>5ch. Timer/Counter<br>16bit Timing pattern gen.<br>Watch-dog timer<br>2ch. Serial comm. port<br>Universal I/O ports | SH7604(SH-2)<br>4kB cache memory<br>Hardware multiplier<br>Hardware divider<br>15ch. Ext. interrupt handler<br>2ch. DMA controller<br>16bit Counter<br>Watch-dog timer<br>1ch. Serial comm. port | Bi-directional two ports of 4bit<br>clock and<br>12bit control signal with strobe<br>(Opto-isolated RS485 interface)<br><br>20bit+Strobe output port<br>(Opto-isolated RS485 interface) |
| Clock | 20MHz (16MIPS) | 28.7MHz (25MIPS) | |
| SRAM | 128kB with zero wait state | 128kB with zero wait state | |
| DRAM | 16MB with zero wait state | 128kB with zero wait state | |
| Dual-ported SRAM | 32kB with one clock wait state | 32kB with one clock wait state | |
| LUT SRAM | 384kB with 20bit U/D counter | | |
| Front panel functions | 16bit Status LED<br>Reset switch | | |
| Bus spec. | VMEbus IEC821 compatible slave interface (A24,D16)<br>VSBbus IEC821 compatible master/slave interface | | |
| Operating condition | Power source: 5V±5% , 3A<br>5V±10%, typ.1.5A (I/O isolation p/s supplied from front connector)<br>Temperature : 0°C~50°C Humidity : 30%~90% (Non-condensing) | | |

## 5. FEATURES OF DPO SOFTWARE

Most of the intelligence of DPO resides in the SH-1CPU, which handles numerous internal/external interrupts and controls many peripherals. In order to reduce any overhead time, the firmware has no OS except for a minimum context switching kernel which arbitrates task priorities when interrupts occur.

When the host CPU on VMEbus receives a command from the CS via TCP/IP, it interrupts the DPO through the dual-ported memory, e.g. dpo-set, dpo-read, dpo-write, dpo-init, dpo-clear, etc. DPO responds to the host on any interrupt. Base and master clocks, similar to T and B clocks from the RC, and all of event signals from the TS are also recognized as interrupts by DPO; Table 3 lists the software functions.

DPO firmware has some optional functions to change smoothly the rf frequency from T clock region to B clock region, to excite current of a magnet from one flat-top region to another and to turn on and off the magnet power supply.

Table 2 External clocks & control signals

| Code | Name | Contents |
|---|---|---|
| - | Master clock | Pattern start signal. It corresponds to repetitive cycle of synchrotron operation, typically ~1Hz. This is also used as rf capture. |
| - | Base clock | 1,200Hz is fundamental clock distributed from PLL.50Hz is also used to 24 phase thyrister trigger timing with zero cross on U phase. |
| - | B+ clock | Incremental B clock for rf. |
| - | B- clock | Decremental B clock for rf. |
| 001 | Start | Command to start pattern output/input to devices altogether. |
| 002 | Stop | Command to stop pattern output/input to devices altogether. |
| 004 | Pause | Command to break temporarily pattern output/input. |
| 008 | Rerun | Command to rerun the pause devices. |
| 010 | T - B | Command to change signal from T clock to B clock. |
| 020 | B - T | Command to change signal from B clock to T clock. |
| 801~ | Select | Command to select any excitation pattern. |

Table 3 Software functions of DPO

| SH-1 CPU for control | SH-2 CPU for calculation |
|---|---|
| Communication with Host CPU of IOC on VMEbus.<br>Communication with SH-2 CPU for calculation.<br>Excution of event signal.<br>VMEbus and VSBbus control.<br>Initialization and placing data on LUT.<br>Smoothing control of pattern.<br>Data output synchronized with external clock. | Communication with SH-1 CPU for control.<br>Calculation of feed-back control or data filtering<br>Smoothing calculation of pattern. |

## 6. DEVELOPMENT SCHEDULE

DPO with basic firmware will be prepared for a performance test by the end of this year. Measurements of response times needed for critical applications e.g. a smooth change from B and T clock of rf, realtime operations of feedback control, etc., will be carried out. The fine adjusument of event control timing in microseconds will have to be checked to use DPO for the TS. System considerations are necessary to specify further details and to establish the best means of utilization. Especially, an optimization of the division between hardware and software is essential, as they are usually contradictory to performance and diversification.

High-speed digital feed-back control with high accuracy is attractive to challenge many technical matters of instabilities in various aspects of synchrotron operation. We expect that the combination of DPI/DPO will be useful to reduce beam ripple or to stabilize beam position by means of high-speed data acquisition and processing.

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1. E.Takada et al., "The HIMAC Synchrotron Control System", Proc ICALEPCS'93. Berlin, Germay, October 1993, pp.40-42, (Nucl. Instr. & Meth A352, ('94)) The article has a typographical error on the name of realtime OS. It should read PDOS, instead of PSOS.
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