The Advanced Photon Source Injection Timing System*

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ABSTRACT

The Advanced Photon Source consists of five accelerators. The injection timing system provides the signals required to cause a bunch emitted from the electron gun to navigate through intermediate accelerators to a specific bucket (1 out of 1296) within the storage ring. Two linacs and a positron accumulator ring operate at 60Hz while a booster synchrotron ramps and injects into the storage ring at 2Hz. The distributed, modular VME/VXI-based injection timing system is controlled by two EPICS-based input/output controllers (IOCs). Over 40 VME/VXI cards have been developed to implement the system. Card types range from 352MHz VXI timing modules to VME-based fiber optic fanouts and logic translators/drivers. All timing is distributed with fiber optics. Timing references are derived directly from the machine low-level rf at 9.77MHz and 351.9MHz. The timing references provide triggers to programmable delay generators. Three grades of timing are provided. Precision timing is derived from commercial digital delay generators, intermediate precision timing is obtained from VXI 8-channel digital delay generators which provide timing with 25ns peak-to-peak jitter, and modest precision timing is provided by the APS event system. The timing system is fully integrated into the APS EPICS-based control system.

INTRODUCTION

The Advanced Photon Source consists of five accelerators: an electron linac, a positron linac, a positron accumulator ring, a booster synchrotron, and the positron storage ring itself. The injection timing system is required to generate all the timing pulses (with the exception of the linacs which have their own timing subsystem) needed to cause bunches to be emitted from the electron gun, accumulated in the positron accumulator ring (PAR), accelerated by the booster synchrotron to 7GeV, and finally injected into selected buckets of the storage ring.

In order to position the bunches in the rf buckets of the three circular machines, the injection/extraction timing pulses for a machine must be synchronized to that machine's rf frequency. The booster and storage ring use the same rf frequency of 351.9MHz. The PAR's fundamental rf frequency is 1/36 that of the storage ring or 9.77MHz. The PAR also uses the 12th harmonic of this frequency to compress its stored bunch. There are 36 rf buckets in the PAR. Since the circumference of the PAR is exactly one wavelength of its fundamental, the 36 rf buckets are accomplished by shifting the phase of the fundamental in 10-degree steps. The booster, which is one-third the circumference of the storage ring, has 432 rf buckets while the storage ring has 1296 rf buckets.

The timing system uses the PAR fundamental rf frequency and the booster/storage ring rf frequency as reference inputs. These inputs are processed by digital circuits to generate timing references which, in turn, are used to trigger digital delay generators. The digital delay generators produce the actual timing pulses. Two grades of digital delay generators are used. For those timing pulses requiring very precise timing, Stanford Research Systems DG535s [1] are used. The DG535s are used for applications such as kicker timing and linac modulator timing. Less demanding requirements are fulfilled with in-house-designed VXI 8-channel digital delay generators. The VXI delay generators digitally count a clock to generate programmed delays. A peak-to-peak jitter of 25ns is obtained when the VXI generator's internal 40MHz clock is used. Nearly all timing signals are transmitted over fiber optic links to their destination.

The Advanced Photon source event system is also an integral part of the injection timing system, but since it is described in detail in another paper [2], it will not be discussed here.

INJECTION TIMING CYCLE

Figure 1 illustrates the APS injection cycle. During storage ring injection, the cycle repeats at a 2Hz rate. Nominal operation requires 24 linac pulses to be accumulated in the PAR at a 60Hz rate. This is followed by a 100ms period in which the PAR bunch is damped and compressed. At about 50 ms after the last bunch is injected into the PAR, the booster synchrotron is commanded to ramp. When the booster reaches the injection energy (~450MeV) about 30 ms after ramping is started, the bunch is ejected out of the PAR and into the booster. The booster then accelerates the injected bunch to 7GeV during the next 220ms, at which point the bunch is extracted out of the booster and into the storage ring.

The injection timing system is required to put the bunch into any of the storage ring's 1296 buckets. This is accomplished by shifting timing reference pulse generation to correspond with the desired bucket. The module that generates timing references for PAR injection uses a PAR rf reference from the rf bucket phase shifter as its internal logic clock. Thus, the generated timing references track the phase-shifted rf. The timing references for PAR extraction, booster injection and extraction, and storage ring injection are shifted digitally via counters that are preset to the desired bucket number and clocked by the booster/storage ring low-level rf.

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PRIMARY TIMING TRIGGERS

Figure 2 is a greatly simplified representation of the timing system. It consists of two input/output controllers (IOCs) separated by about 300m. One IOC, iocinjtime, is located in the injection control room, while the other, iocmtime, is located in the main control room. Iocinjtime controls timing for linac triggers, PAR injection/extraction, booster injection, and the associated beam transfer lines. Iocmtime controls booster extraction, storage ring injection, and the associated beam transfer line. Each IOC is VME based with an attached VXI crate and GPIB bus. The IOC's processors run the EPICS control system software under vxWorks. All timing parameters are controlled through EPICS graphical control screens.

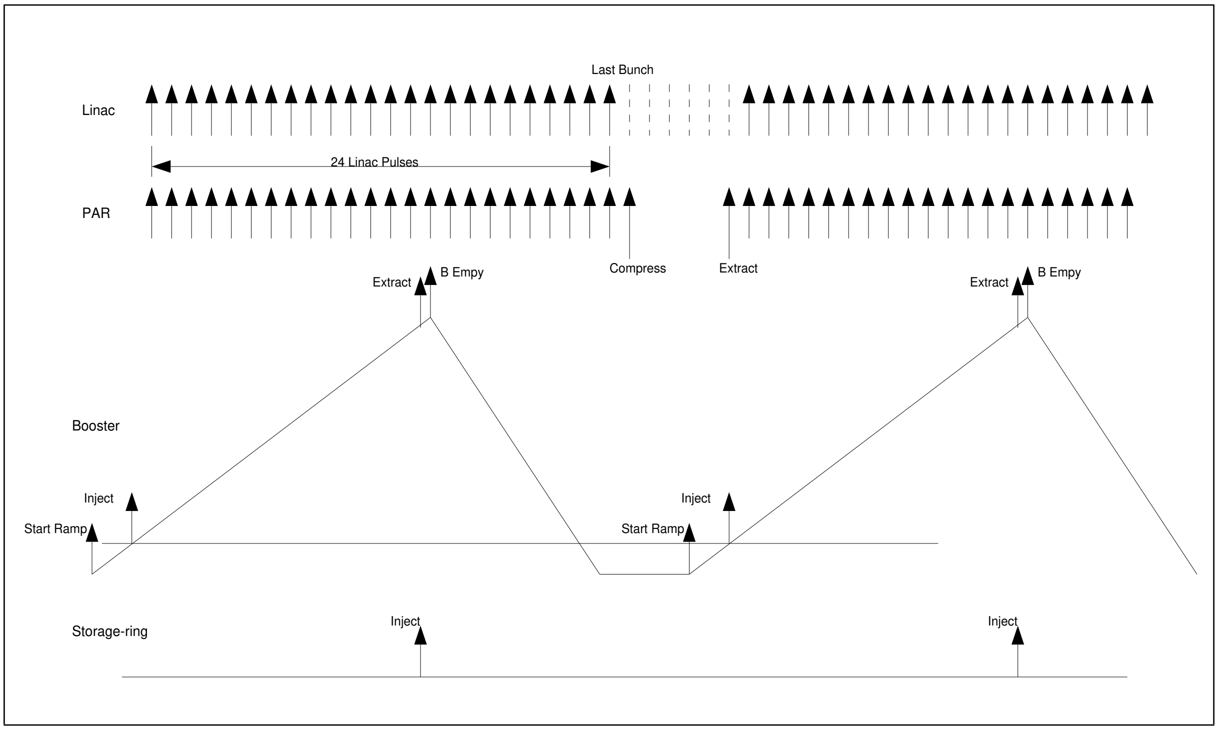

Figure 1 The APS Injection Timing Cycle

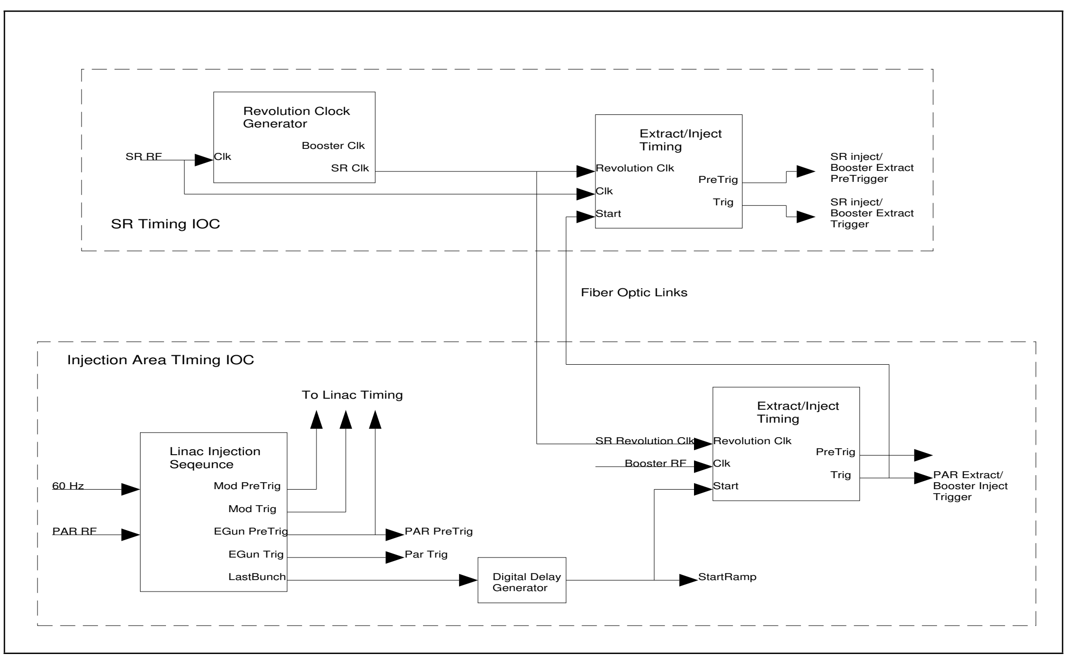

Figure 2 Injection Timing System Block Diagram

Each IOC generates many timing signals to control kickers, septa, diagnostics, etc. Most of these signals are generated by digital delay generators that are triggered by timing fiducials. The timing fiducials are derived from three primary references: the 60Hz line frequency, the PAR fundamental frequency, and the booster/storage ring rf frequency. The booster/storage ring rf frequency is synchronously counted by the Revolution Clock Generator module in iocmtime to produce revolution clocks for the booster synchrotron and the storage ring.

Timing fiducials for linac to PAR are generated by a Linac Injection Sequence module which is described in greater detail below. The fiducials are: linac modulator pretrigger (to time modulator charging), linac modulator trigger, linac electron gun (egun) pretrigger, PAR pretrigger (controls pulsed supply PFN charging), PAR trigger (times pulsed magnet firing) and last-bunch which provides a timing reference for things that happen during the PAR compress and extract period.

An injection cycle begins with the generation of egun pretrigger/trigger timing references. A pretrigger occurs 1/60th of a second before a trigger. The pretrigger triggers a set of digital delay generators that commands the PAR pulsed magnet power supplies to charge their PFNs. The egun pretrigger also sets up the linac timing subsystem to trigger the egun on the next modulator trigger. The egun trigger timing fiducial triggers a set of digital delay generators that generates PAR pulsed magnet power supply discharge commands. The egun pretrigger and trigger timing fiducials are synchronized to the first PAR rf cycle zero crossing following a 60Hz line zero crossing. Thus, the egun pretrigger and trigger are synchronized to both the PAR rf and the 60Hz line frequency.

A last bunch timing fiducial is generated coincident with the last egun trigger pulse in the sequence. This signal provides a timing reference for things that are to occur after the PAR is filled, such as turning on the PAR 12th harmonic rf to compress the bunch and commanding the PAR extraction and booster injection pulsed magnet power supplies to charge their PFNs. The last bunch is also used to trigger a digital delay generator which generates a start ramp timing fiducial. Start ramp initiates the booster synchrotron ramp cycle.

When a start ramp occurs, the timing system counts a preset number of storage ring revolution clocks to determine when to generate the PAR extract/booster inject timing trigger. This timing reference triggers a number of digital delay generators which produce discharge commands to the PAR extraction and booster injection pulsed magnet power supplies. This timing reference also triggers the PAR-to-booster beam transfer line timing generators.

The booster inject timing trigger is transmitted via a fiber optic link to iocmtime which controls booster extraction. The booster injection trigger causes iocmtime's Extract/Inject Timing module to begin counting storage ring revolutions. This module is loaded with the number of revolutions required for the booster to accelerate the bunch to 7 GeV. The acceleration period is approximately 220 ms. About 40 ms before booster extraction, the Extract/Inject Timing module generates the booster extract/storage ring inject pretrigger. This timing reference triggers digital delay generators that command the booster extraction and storage ring injection pulsed magnets to charge their PFNs. At 350 microseconds before booster extraction, the module generates the trigger timing reference which triggers digital delay generators that produce discharge commands for the booster extraction and storage ring injection pulsed magnets. Beam transfer line diagnostics are also timed relative to this trigger signal. Upon bunch extraction, the booster is commanded to ramp down in preparation for the next cycle.

Different storage ring buckets are filled by shifting the timing references generated by the Extract/Inject timing modules in the two timing IOCs. Each of these modules counts storage ring rf cycles relative to the revolution clock to select different buckets.

LINAC INJECTION SEQUENCE

Figure 3 show a greatly simplified block diagram of the Linac Injection Sequence trigger (LIST) module. This VXI module generates timing references that are used to control linac triggering and PAR injection. It accepts the 60Hz line frequency and PAR rf frequency as inputs. The internal logic is completely synchronous and uses the PAR rf input as the clock.

The module uses two 30-bit synchronized shift registers to generate two sequences of pretrigger and trigger timing references. One sequence times the linac modulators while the other times egun triggers and PAR injection. Any 30-bit pattern may be specified for either the modulator or egun trigger sequences. The bit patterns are shifted out at the 60Hz rate and repeated at a 2Hz rate. Each shift register has an associated sequence length counter which determines the end of a sequence. The pretrigger and trigger outputs are 1/60th of a second apart and always occur in pairs.

All outputs from the LIST module are synchronized to the first PAR rf cycle zero crossing following a 60Hz line zero crossing. Although not shown in the simplified diagram, the LIST module contains a delay counter which can shift the timing of all outputs relative to the 60Hz line by an even number of PAR rf cycle to a maximum of 128k.

EXTRACT/INJECT TIMING MODULE

Figure 4 shows a simplified block diagram of the VXI module which generates the pretrigger and trigger timing references for PAR extraction, booster injection/extraction, and storage ring injection. One of these modules is located in both iocinjtime and iocmtime.

The module's internal logic is completely synchronous to minimize timing errors due to logic propagation delay drifts. The module uses the 352MHz booster/storage ring rf as its internal clock. A 16-bit presettable counter counts rf cycles after the occurrence of the storage ring revolution clock. This counter is preloaded with the desired bunch number. When the bunch number is reached, the counter generates a bunch select signal which is connected to the count inputs of two additional presettable counters—

the turns counter and the pretrigger delay counter. These two counters begin counting bunch selects upon occurrence of the start input. The turns counter is preloaded with the number of turns to occur between start and the pretrigger timing reference out. The pretrigger delay counter is preloaded the number of turns desired between the generation of pretrigger and trigger. Load bunch is an external input which is driven by a signal that is timed (via a digital delay generator) to update the bunch select register with a new value (written by the IOC) between timing cycles.

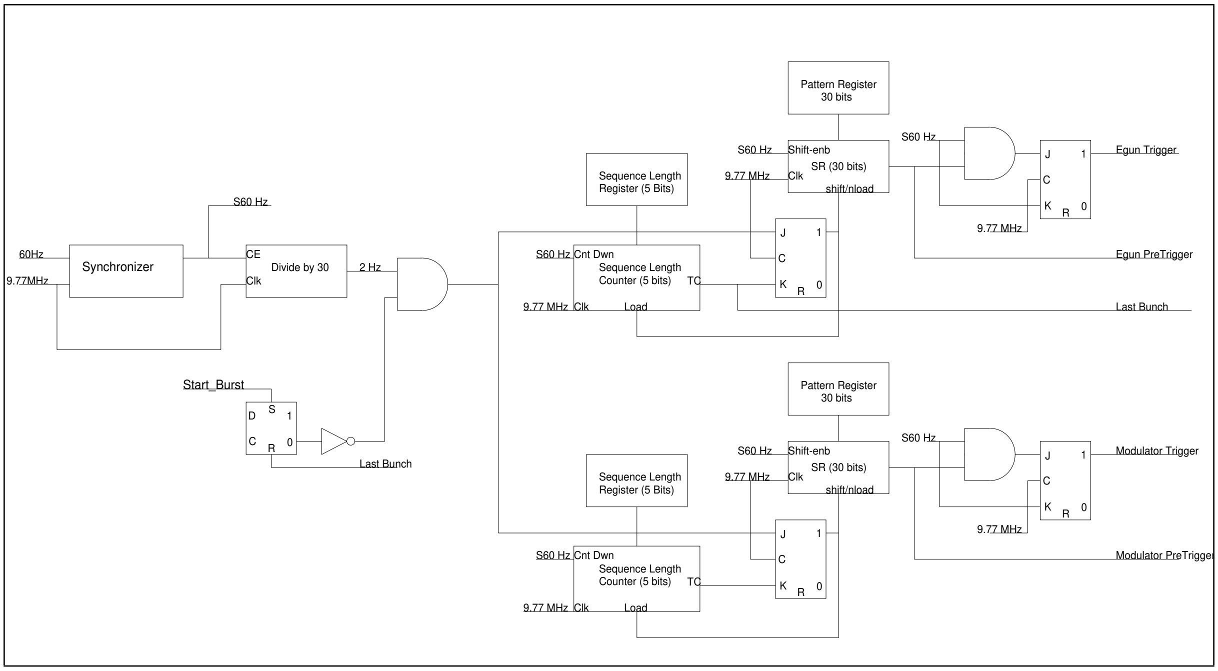

Figure 3 The Linac Injection Sequence Trigger Module Block Diagram

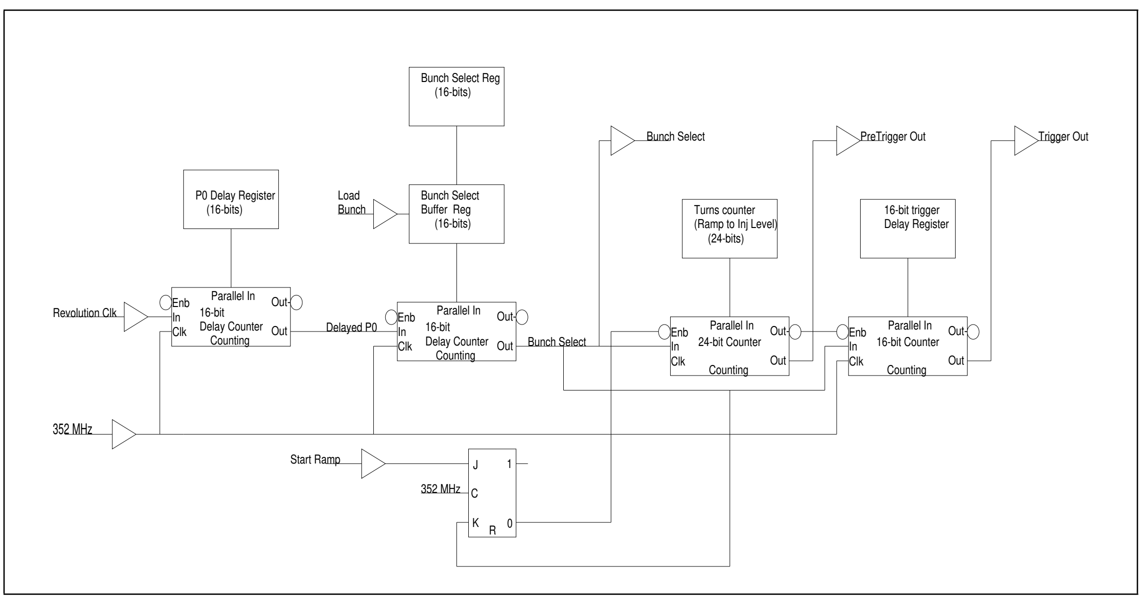

Figure 4 The Extract/Inject Timing Module Block Diagram

The operator need only set things such as desired storage ring bucket number and booster ramp time. The IOC processors calculate the proper numbers to load into the Extract/Inject Timing modules. As mentioned previously, the module uses the 352MHz low-level rf as a clock for its synchronous logic. We have, however, successfully tested the module with input clocks of up to 490MHz.

REVOLUTION CLOCK

The revolution clock VXI module produces revolution clocks for the booster and the storage ring. This module uses synchronous counters to divide the 352MHz booster/storage ring rf reference by 432 to obtain the booster clock. The booster clock is in turn divided by three with another synchronous counter to produce the storage ring revolution clock. The module also has an input for the PAR 9.77MHz fundamental rf. This input is obtained from a source ahead of the PAR bucket phase shifter and is used to determine which of the 432 booster and 1296 storage ring buckets will be bucket “0.” Upon command from the IOC, the revolution clock counters are synchronously reset at the next 9.77MHz zero crossing. Under normal circumstances, this resyncing of the revolution clocks need only be done at system initialization time.

VXI DIGITAL DELAY GENERATOR

Figure 5 shows a block diagram of the 8-channel VXI digital delay generator developed for general-purpose timing. The eight channels have independent programmable selection of clock source and trigger source. Each channel may be triggered from any of the VXI TTL trigger lines or from one of four front panel trigger inputs. The clock source may be the internal 40MHz clock, the internal clock divided by 2 or 4, or the external clock input.

The counters for each channel are contained in an individual programmable logic device (PLD). Thirty-two bits are available for pulse width/delay determination. The number of bits assigned to width and delay is determined by how the PLD is programmed. We have three standard configurations: 8-bit width x 24-bit delay, 16-bit width x 16-bit delay and 24-bit width x 8-bit delay. A channel’s delay and width range depend on which type of PLD is socketed for that channel. The 8-bit width x 24-bit delay is used most frequently. With this configuration, pulse widths of up to 6.4 microseconds and delays of up to 419 milliseconds with a resolution of 25 nanoseconds are possible.

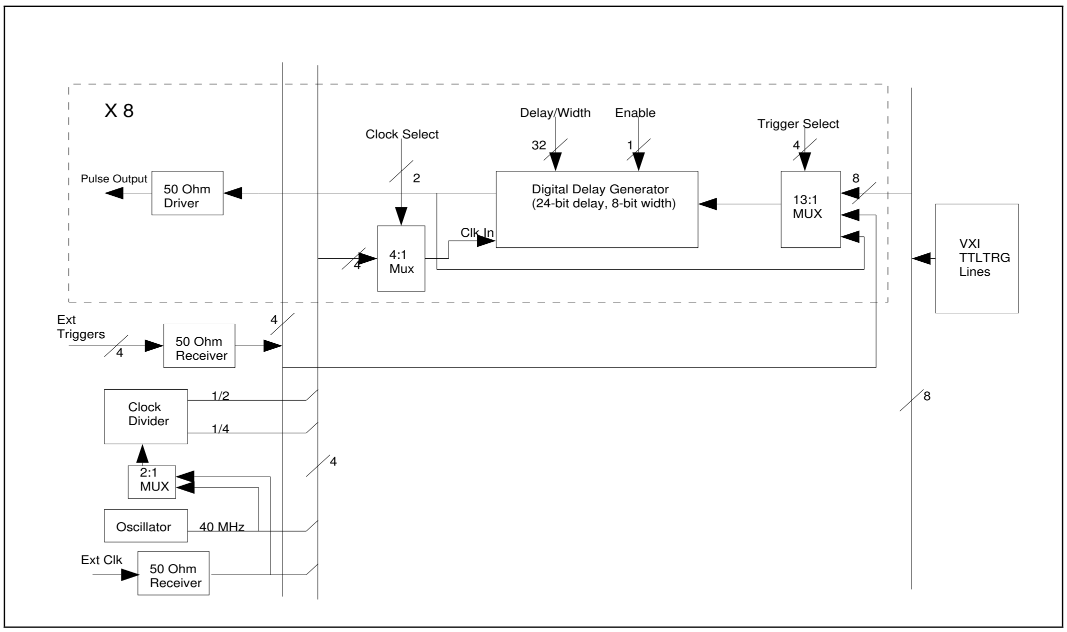

Figure 5 Eight-channel VXI Digital Delay Generator

OTHER MODULES

All together about 40 different VME and VXI modules have been designed to implement the APS injection timing system. Other modules include: VME video sync generator, VME revolution clock counter/trigger, fiber-optic transmitters and receivers, fanouts, and logic-level converters. All the modules are plug and play and are supported by EPICS. VME fanout and logic-level convertor modules use the VME backplane for power only; i.e., they have no programmable features.

CONCLUSION

The timing system has been in place for nearly two years. Although a good deal of effort was expended initially to determine timing requirements, many additional ones arose as the systems began to come on-line. The timing system’s modularity made it possible to respond to all these new requirements in a timely fashion.

REFERENCES

[1] Stanford Research Systems, Inc., Sunnyvale, Ca.

[2] F. R. Lenkszus, R. Laird, “The Advanced Photon Source Event System,” these proceedings.