The VEPP-4 Timing System

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Abstract

The VEPP-4 timing system provides:

- precision timing with resolution of 0.2 ns in the range of 6.5 μs (generation of references required to transfer bunches from one accelerator to the other and to fit RF systems),
- medium precision timing with resolution of 0.1 μs in the range of 6.5 ms to synchronize pulsed devices (magnets, RF systems, injection-extraction elements) for ramping, extraction, and injection of bunches,
- synchronization of the application programs (resolution of 10 μs in the range of 1 sec) in each computer and between computers.

There are no data links to synchronize activities across the facility. The timing system is based on using a set of digital delay generators that are used for generating references to operate pulsed equipment and to control application programs.

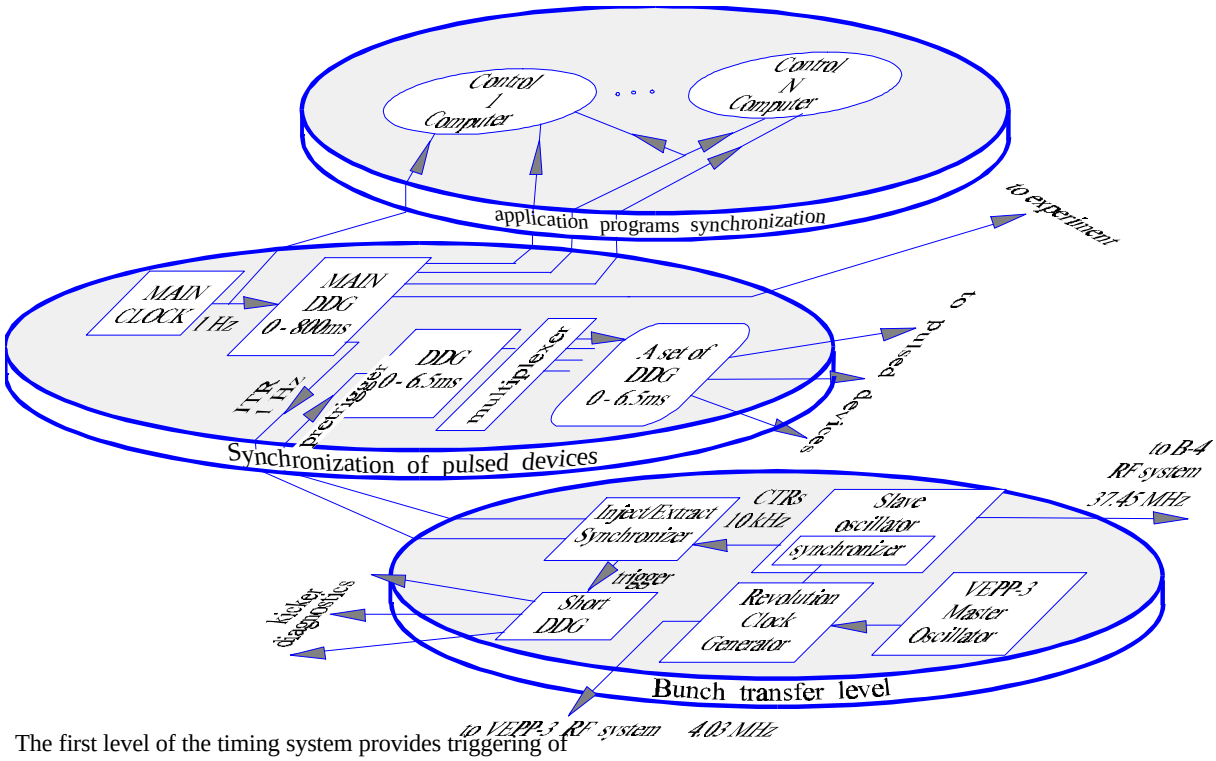
Timing references are derived from the electronics for controlling RF systems. Modest precision timing and synchronization of programs are provided by digital delay generators (DDGs).

The control of the timing system is distributed between four computers and is integrated into the VEPP-4 control system [1]. All timing signals are transmitted through coaxial cables.

1 Introduction

The VEPP-4 facility consists of four components: collider VEPP-4M with 365 m circumference, storage ring VEPP-3 with 75 m circumference, the pulsed beam transportation channel between the collider and the storage ring, and the injector to VEPP-3.

There are three levels of the VEPP-4 timing system: synchronization of bunch transfer, synchronization of the injector and transfer lines pulsed devices (charging and firing), and synchronization of application programs (see Fig. 1).



The first level of the timing system provides triggering of

Figure 1 Diagram of the timing system

pulsed injection/extraction devices of linear accelerator LINAC and synchrotron B-4 (which are the parts of the injector), storage ring VEPP-3, and collider VEPP-4M.

The second level provides synchronous triggering and operation of pulsed devices. It is based on using in-house developed Digital Delay Generators (DDGs) which provide timing with resolution from 100 ns up to 10 μs in the range between 6.5 ms and up to 838 ms.

Application program synchronization level of the timing system provides generation of interrupts in the control computers in response to external input references to synchronize different control applications, both in a one computer and different computers.

2 Bunch transfer synchronization

The Bunch Transfer Synchronization System consists of two subsystems: the first subsystem synchronizes the bunch transfer from synchrotron B-4 to storage ring VEPP-3, the second subsystem provides the extraction of bunches from the storage ring and the injection into the collider. Both subsystems are based on in-house developed electronics. They use low level reference signals of 4 MHz (VEPP-3 storage ring), at 181 MHz (VEPP-4M collider), and at 37.4 MHz (synchrotron B-4). There are 222 RF buckets in VEPP-4M, 18 RF buckets in VEPP-3, and 1 RF bucket in B-4. Fig. 1 in the bottom level shows a simplified block diagram of the synchrotron/storage ring subsystem. The electronics of the subsystem includes: VEPP-3 master oscillator, B-4 slave oscillator, Injection/Extraction Synchronizer (IES), Short Digital Delay Generator (SDDG) with 0.2 ns resolution, Revolution Clock Generator (RCG).

The signal from the phase detector of B-4 synchronizer controls the slave oscillator, so that

$\frac{f_{sy}}{f_{sr}} = \frac{N}{402}$, where f_{sy} is the revolution frequency of the synchrotron, f_{sr} is the revolution frequency of the storage ring, $N = 3760$ and may be changed in the range of 3%.

The Clock Timing References (CTRs) are derived from two primary references: 4 MHz of the storage ring and 37.4 MHz of B-4 synchrotron revolution frequency. CTRs mark the moments of time when the transfer of bunches from B-4 to VEPP-3 is favorable. The repetition rate of CTRs is ≅ 10 kHz. In B-4 RF frequency control process, the slave oscillator changes the parameter N, so that CTRs occur frequency is a constant.

IES is triggered by the Initial Timing Reference (ITR) from the second level of the timing system (see Fig.1). The first CTR pulse (which comes after each ITR) generates pretrigger reference, which starts a set of DDGs of the second level. DDGs produce references to discharge pulsed generators of the injector and of the transfer line between VEPP-3 and VEPP-4M. The 64-th CTR pulse after the pretrigger reference actuates the SDDG. SDDG outputs enable the kickers and diagnostics.

The second part of the Bunch Transfer Synchronization System for extraction from VEPP-3 and injection to VEPP-4M is based on the same principles as the first part. It uses VEPP-3 and VEPP-4M fundamental RF (8 and 181 MHz).

3 Pulsed devices synchronization

The pulsed devices synchronization system consists of two parts: injector and VEPP-3 - VEPP-4M transfer beam line subsystems.

To generate trigger timing references a set of more than 20 DDGs is used. DDG is a CAMAC-embedded module with eight 16-bit synchronized shift registers. Each shift register has a sequence length counter which determines the end of the sequence. The outputs are pulses of +15 V amplitude and of 1 μs width with 1 Hz repetition rate. All channels of the module are started from one trigger input and have a maximum delay of 800 ms.

Fig. 1 in the middle level shows a simplified block diagram of the injector pulsed devices trigger system.

4 Application programs synchronization

There are three computers to control pulsed systems: two computers to control the injector and one computer to control transfer beam line from VEPP-3 to VEPP-4M [1]. About 15 application programs are used simultaneously in these computers.

The main instrument to synchronize applications in one computer or several computers is Peripheral Interrupt (PINT) method. The PINT register CAMAC module produces LAM-signal after occurrence of the input reference in any of its 16 inputs. The delay between occurrence of any input reference and start of any application waiting for this event is about 300 μs.

There is a possibility to generate PINTs from application programs by using PINT generator CAMAC module, as well as by using a special command for the operation system.

Fig. 2 shows a greatly simplified diagram of a PINT sequence in the injector control computer.

PINT 1 indicates the occurrence of the reference from MAIN CLOCK generator. After that, all control applications complete data acquisition and exchanges. When a massive of data is compiled, the main control program (Resident Executive Program [1]) produces PINT 8 that initiates other applications to get new data about the last operation cycle. PINT 2 is produced by the main DDG to initiate measurements of voltages on pulsed generators banks. The time interval of this procedure is about 100 ms. PINT 3 occurs in the moment of the pretrigger reference occurrence. This timing reference simultaneously triggers a number of modules to measure pulsed magnetic fields and coil currents. PINT 4 initiates application programs to read pulsed measurements and calculate parameters of bunches and generators.

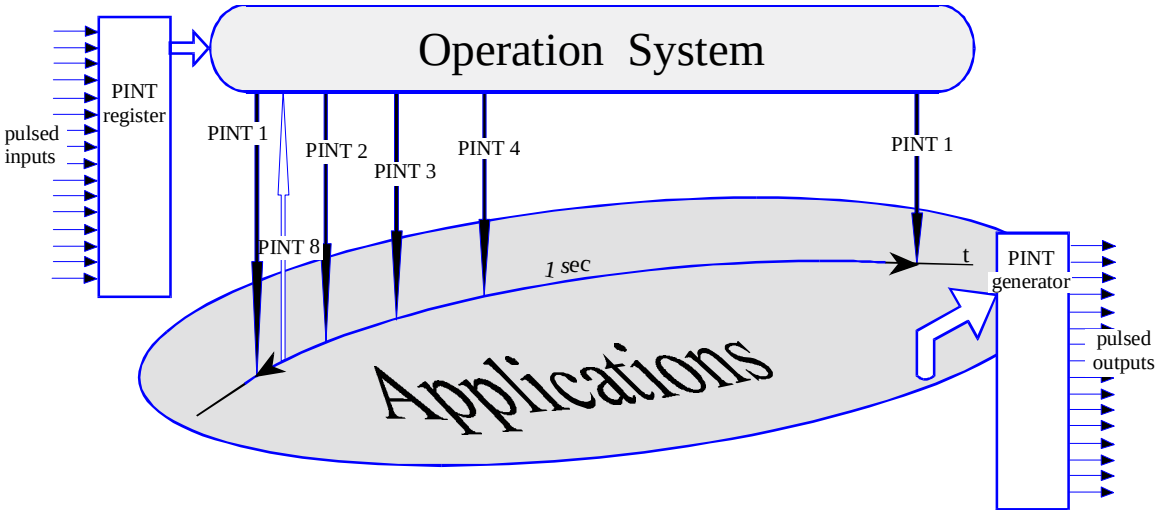


Figure 2 Diagram of a PINT sequence in the injector control computer

5 Conclusion

The timing system is integrated into VEPP-4 control system. It is responsible for all new requirements and permits to generate references at any moment of operation.

The ability to control application programs upon occurrence of timing events (using PINT method) is very useful.

References

[1] A.Aleshaev, et.al. VEPP-4 Control System, ICALEPCS'95, Chicago, USA, p.799, F-PO-2 .