Development of broadband X-ray and Gamma-ray Detector based on Silicon Drift Detector and Scintillator

K.Yamaoka[1], Y.Arai[1], T.Doshida[1], A.Yoshida[1], A.Pahlke[2], T.Takahashi[3], H.Ikeda[3], H.Kato[4], K.Mori[5]

[1]Aoyama Gakuin University, [2]KETEK GmbH, [3]Institute of Space and Astronautical Science (ISAS/JAXA), [4]RIKEN (The Institute of Physics and Chemical Research), [5]Clear Pulse

We propose a next-generation gamma-ray burst (GRB) detector combining the silicon drift detector (SDD) array and scintillators with broadband coverage (0.5 - 1000 keV), high energy resolution (2 - 10 %) and high time resolution (~ μs). In this detector, photons with lower energy than 40 keV are detected directly with SDDs, while high energy photons above 40 keV interacts with scintillators, which produces UV light in the scintillators so that it can be also readout by SDD with a high quantum efficiency. We constructed a single-channel proto-type model using KETEK SDD with a detection area of 100 mm^2 and BGO crystal. The signals from both detectors are clearly separated by the double integration method. Obtained energy resolution (FWHM) was 1.98 % @ 32 keV with the SDD, while 6.52 % @ 662 keV with the BGO at –30 ℃. As the next stage, we develop an 8-channel analog ASIC to readout signals from multi-channel SDD array ,which achieves larger effective area. In this session, we also report the developmental status of this ASIC.

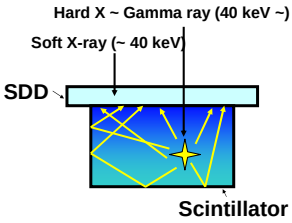
1. Introduction

Gamma-ray Burst (GRB) Scientific Problem

- Broad-band study of GRBs (Classical GRB, X-ray Rich GRB, X-ray Flash)
- Study for formation environment of GRBs
- Iron-features in the prompt emissions

Performance Demanded from Detector

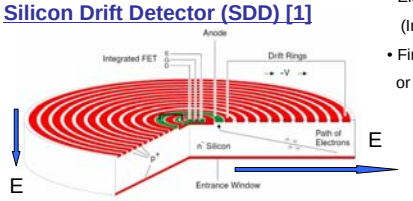
- Broad-band coverage (0.5 ~ 1000keV)
- High energy resolution (2 – 10%)
- High time resolution (~ μs)



⇨ **A combination of Silicon Drift Detector (SDD) array and Scintillator for the next-generation GRB detector.**

2. Detector Design

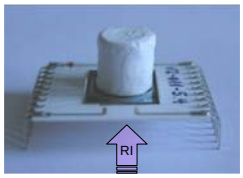
Silicon Drift Detector (SDD) [1]



- Electron is drifted to central small anode (Independent of active area)
- First-stage FET is integrated in the device or very close to the device

⇨
- ➢ Low noise performance
- ➢ High energy resolution
- ➢ room temperature device

SDD + BGO Hybrid Detector



We constructed a proto-type model using KETEK SDD and BGO crystal !!

Ketek Vitus SDD	BGO crystal
• Effective area : 100mm^2	• Saint Gobain ϕ=10mm t=10mm
• Depletion layer : 260μm	• Painted $BaSO_4$ for reflector
• Capacitance : ~ 200pF	• 7.5% @ 662keV with PMT
• External fast-stage JFET	
• 194eV @ 5.9keV (-35℃)	

SDD and BGO were coupled with optical grease

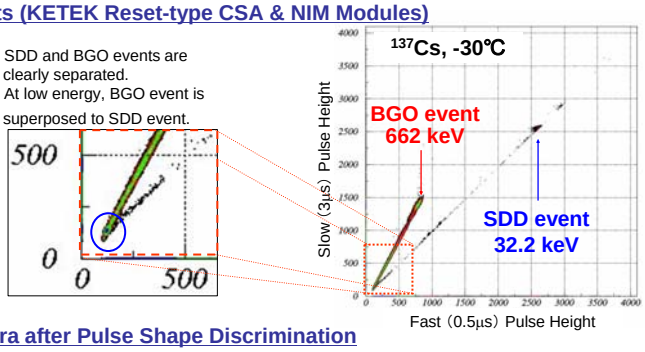
3. Experimental Results

Double Integration Method [2]

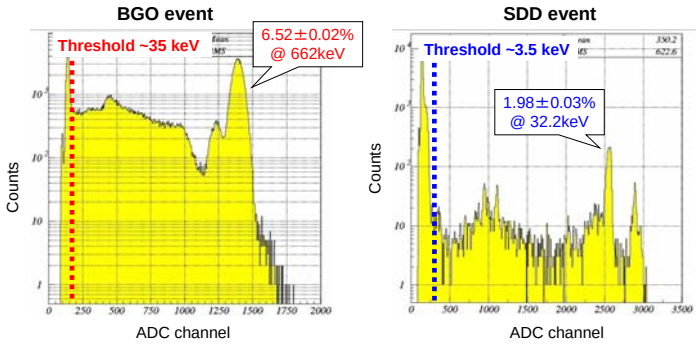
The SDD event has a short rise time of ~ 100 ns, while the BGO event has a longer rise time of ~ μs. Use shaping amps with two time constants of 0.5μs (Fast) and 3.0μs(Slow) for event discrimination. 2-dimensional pulse height distributions in slow and fast shaper outputs.

2-Dimensional Pulse Height Distribution with commercially available circuits (KETEK Reset-type CSA & NIM Modules)

- SDD and BGO events are clearly separated.
- At low energy, BGO event is superposed to SDD event.



Spectra after Pulse Shape Discrimination



Energy Resolution at 662keV	
BGO + PMT	7.48±0.05 %
BGO + SDD	**6.52±0.02 %**

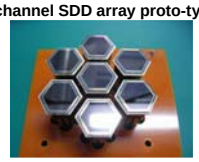
SDD detectable energy threshold : **~ 3.5 keV**
For better separation, we can change rise time by varying electric field gradient in SDD (Now trying).

4. 8-channel analog ASIC

Development of 8-channel Analog ASIC

- ✓ High-speed readout of signals from multi-channel SDD array
- ✓ Miniaturization and lightening of readout system
- ✓ Event discrimination by double integration method

7-channel SDD array proto-type

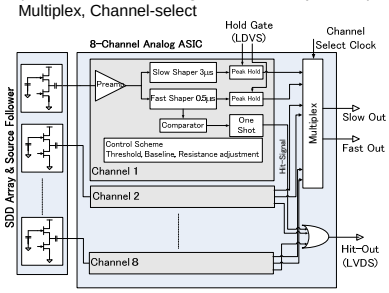


Effective area : 756mm^2

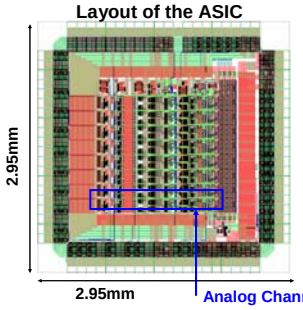
Circuit Configuration

➢ **Analog channels**
Preamplifier
Shaper (Fast:0.5μs, Slow:3μs)
High-resistance circuit, Comparator, Peak-hold

➢ **Control Scheme**
Shift register
(Threshold, Baseline, High-resistance adjustment)
Multiplex, Channel-select

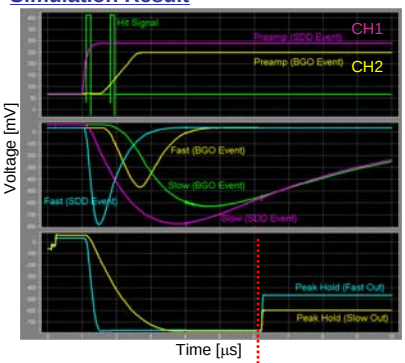


Layout of the ASIC



Fabrication process	TSMC 0.35μm CMOS
Options	4-metal, 2-poly
Power consumption	33mW
Power rail	±1.65V

Simulation Result



Channel select clock is input at this timing (~200kHz).

1. Input the following test pulse
   SDD event : Rise time = 10ns, -2.2mV (CH1)
   BGO event : Rise time = 1μs, -1.8mV (CH2)
2. Preamp output is input to the Fast and the Slow shaper.
3. Fast-shaper output is input to comparator, and hit-signal is generated comparing with threshold voltage.
4. BGO event has a long rise time (1μs), so Fast-shaper output is lower than Slow-shaper output.
5. Both the peak of shaper outputs are holded and output to slow-out and fast-out.
6. The 8 analog channels of the chip are multiplexed to a single analog output. Hence it is possible to readout the signals from all channels by inputting a select-clock.

5. Conclusions

- We constructed a proto-type model of GRB detector using SDD and BGO.
  Energy Coverage : 3.5 ~ 40 keV (SDD) , 35 keV ~ 2 MeV (BGO)
  Energy Resolution : 1.98±0.03 % @ 32 keV (SDD), 6.52±0.02 % @ 662 keV (BGO)
- SDD and BGO event were clearly separated by double integration method. For better separation, we trying to change the rise time by varying electric field gradient in SDD.
- We develop an 8-channel analog ASIC to readout the multi-channel SDD array.
  The simulation result is excellent.
  This ASIC is available on Jun. 2007, and is being tested now.
- In a future, we will combine SDD and $LaBr_3$(Ce) scintillator. [3]
  (Saint Gobain ϕ = 6 mm, t = 6 mm Energy Resolution : 3.1 % @ 662 keV by PMT)

References

[1] P.Lechner et al., Nucl. Instrum. Methods, vol.A 458, pp.281—287, 2001
[2] M.Marisaldi et al., IEEE Trans. Nucl. Sci., vol.51, pp. 1916—1922, 2004
[3] E.V.D. van Loef et al., Applied Physics Letters. vol.79(10), Sept.2001, pp.1573—5